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Fractional-N PLL for RF Applications with Adaptive Intelligent Controller and AVLS Divider

Saeed Pourakbari [1•], Hadi Jahanirad [1]

Abstract- This paper presents the design and simulation of a high-performance fractional-N phase-locked loop (PLL) frequency synthesizer with a 60 kHz bandwidth, operating within a frequency range of 2.4 GHz to 2.5 GHz. The design integrates advanced features such as a sigma-delta modulator configured in a 1-1-1 MASH architecture and a fractional divider, both implemented with intelligent control circuits to precisely determine the division ratio. These innovations aim to reduce delay and power consumption while enhancing phase noise performance and ensuring robust system stability. The fractional divider is a critical component of the PLL, enabling frequency division into fractional values with high precision. By incorporating intelligent control circuits, the design achieves accurate adjustments to the division ratio, contributing significantly to the overall reliability and efficiency of the PLL. Additionally, integrating advanced modulation and filtering techniques further optimizes the loop's performance by suppressing unwanted noise and ensuring stability under varying conditions. Simulation results demonstrate the effectiveness of the proposed design, achieving a fast frequency lock time of approximately 3 µs, a stable phase margin of 45 degrees, and an impressive phase noise performance of -148.13 dBc/Hz at a 1 MHz offset. Furthermore, the system's total power consumption is only 2.36 mW, highlighting its exceptional balance between power efficiency and high performance.

Index Term*: *Fractional-N Frequency Synthesizer, Fast locking, Divider, Sigma-Delta Modulator, Delay Locked Loops, AVLS.

I. INTRODUCTION

Phase-Locked Loops (PLLs) are essential control systems in electronics and telecommunications, enabling the generation of output signals synchronized in phase with input references. They are critical for applications such as frequency synthesis in wireless communication systems, GPS receivers, and high-speed data links, where precise frequency generation, low phase noise, and efficient power usage are paramount [1], [2]. However, traditional integer-N PLLs face significant limitations in achieving fine frequency resolution at high output frequencies. These include the necessity for small reference frequencies (Fref) to enable narrow channel spacing, which in turn requires large division ratios (N), leading to increased circuit size, higher power consumption, prolonged lock times, and elevated phase noise due to the amplification of in-band noise by the factor N [3], [4].

To mitigate these issues, Fractional-N PLLs have emerged as a superior alternative, allowing non-integer division ratios by dynamically switching between N and N+1, thereby achieving finer frequency steps with higher Fref, reduced N values, wider loop bandwidths, faster locking, and lower phase noise [5], [6]. Despite these advantages, Fractional-N architectures introduce challenges such as fractional spurs from periodic division patterns and quantization noise from delta-sigma modulators (DSMs), which can degrade spectral purity and overall performance if not properly managed [7], [8]. The core of a fractional-N synthesizer lies in its feedback loop divider and the associated accumulator circuit. The accumulator receives an n-bit DC input, generating an overflow bit in each cycle. As a result, the divider divides the VCO output by N for a specified number of cycles and by N+1 for others, achieving the desired fractional division [3], [4].

At this stage of analysis, we can compare integer and Fractional-N synthesizers. Fractional frequency dividers offer finer frequency resolution, and Fractional-N synthesizers typically operate with a higher reference frequency than integer dividers. This enables them to achieve at least double the bandwidth of integer dividers, allowing the PLL to lock faster. Additionally, the higher reference frequency requires a smaller division ratio, which in turn reduces phase noise [3], [4].

A comprehensive review of prior studies reveals ongoing efforts to enhance Fractional-N PLL performance. Early works emphasized basic architectures for spur reduction, such as using higher-order DSMs to shape quantization noise

[1] Department of Electronics and Communication Engineering, University of Kurdistan, Sanandaj, Iran.
• Corresponding author: saeed.akbarilisar@uok.ac.ir

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out of the band of interest [1], [5], [6], [7], [8], [9], [10]. For instance, foundational analyses explored delta-sigma fractional-N PLLs for frequency synthesis, focusing on noise shaping and modulator designs to minimize spurs [6], [8]. Other early contributions included systematic design methodologies for multi-modulus dividers in low-power applications and simulation of fractional-N sigma-delta PLLs to address phase noise and spurious tones [6], [11].

More recent advancements have built on this foundation, targeting improvements in jitter, power efficiency, locking speed, and integration in advanced processes. For example, in 2018, Li et al. presented a 5.7–6.0 GHz CMOS PLL in 130 nm technology with low phase noise and a -68 dBc reference spur, achieved by reducing charge pump mismatch and optimizing the loop filter, resulting in a reference spur improvement of at least 17% and the lowest phase noise among comparable designs [4]. In 2022, Jo et al. developed a low phase-noise dual-band (2.4 and 5.8 GHz) frequency synthesizer in 180 nm CMOS for RF wireless charging, incorporating a class-C VCO and bias-controlled charge pump, achieving figures of merit (FoM) of -197 dB at 2.4 GHz and -202.8 dB at 5.8 GHz, with phase noise of -125.8 dBc/Hz at 1 MHz offset and 13.4 mW power consumption, outperforming other PLLs in the same process [12].

Further progress includes a 2024 design by Shehab et al. of a delta-sigma-based fractional-N PLL at 2.4 GHz for WLAN in IEEE 802.11 standards, emphasizing simulation and optimization for wireless local area networks [13]. Ali et al. in 2019 proposed a fast-locking technique for PLLs based on phase error cancellation, reducing lock time significantly [14]. Wang et al. in 2020 introduced a programmable frequency divider with full modulus range and 50% duty cycle [15], while Kazeminia in 2020 explored a frequency-range enhanced delay-locked loop using varactor-loaded delay elements [16]. Sahani et al. in 2022 presented a dual-loop ADPLL with foreground calibration and 6 ps resolution flash TDC in 180 nm CMOS, achieving 1 µs lock time [17].

A 2025 study reviewed progress in low-jitter fractional-N PLLs, highlighting techniques like multipath feedback for quantization error compensation and high-gain phase detectors with DTC range reduction, achieving RMS jitter as low as 37.7 fs and figures of merit up to -254.6 dB [18]. Similarly, a 2024 design presented a low-power, low-phase-noise PLL for WLAN/WiFi, using a dual-symmetric VCO and improved PFD/CP, attaining phase noise of -111.7 dBc/Hz at 1 MHz offset with 7.14 mW consumption [19]. A 2024 compact fractional-N PLL in 12 nm FinFET with a single-ended ring VCO featured variable resistor matrices for tuning, resulting in 2.702 ps RMS jitter at 5.76 GHz and power below 7.5 mW across 2.24–6.72 GHz [20]. In 2024, a power-efficient fast-locking PLL employed TDC-aided adaptive control, auxiliary CP, and switchable ring-VCO modes to reduce locking time while optimizing phase noise and power, achieving 1.11 µs lock time, -98.07 dBc/Hz at 1 MHz, and 1.86 mW power [21]. A 2021 approach for ultra-fast chirps in FMCW radar used offset currents and capacitor arrays in fractional-N PLLs to minimize settling times and phase noise [22]. Recent surveys and presentations underscore these developments. A 2025 comprehensive survey on PLL IC design traces evolution from 180-nm CMOS to FinFET nodes, noting fractional-N advancements like a 12.5-GHz type-I sampling PLL with 58-fs jitter and ring-DCO-based designs with DTC range reduction [34]. Trends also include DTC-assisted architectures for low spurs and fast locking (e.g., <100 fs jitter), emphasizing digital calibrations and multi-core VCOs for wireless standards like WiFi 7 and 5G [18], [23].

Despite these advances, gaps remain in balancing ultra-low power (below 3 mW), exceptional phase noise (better than -140 dBc/Hz at 1 MHz), and sub-5-µs lock times in compact 0.18-µm CMOS implementations for applications like 2.4-2.5 GHz wireless systems. Prior works often trade off power for noise performance or require advanced nodes for jitter reduction, limiting accessibility.

This work presents a novel Fractional-N PLL design that incorporates a third-order sigma-delta modulator, AVLS-based D flip-flops for the divider, a multi-modulus divider with CML and CMOS logic, an intelligent control circuit for division ratio adjustment, and a MASH 1-1-1 sigma-delta modulator structure. The design operates in the 2.4 GHz to 2.5 GHz range with a reference frequency of 20 MHz, achieving low phase noise, reduced power consumption, and fast lock time through optimized filter design and advanced techniques.

The novelties of the proposed method include the integration of the AVLS technique in D flip-flops to minimize power and delay, using CML logic in the initial divider stage for high-speed operation, and an intelligent 32-to-5 bit converter for precise control of division ratios. Compared to other studies, such as [24] which designs a fractional-N PLL synthesizer with 200 kHz bandwidth for satellite and radar applications, achieving a 3 µs lock time and 45° phase margin but without detailed phase noise or power metrics reported in the abstract, the proposed design advances wireless applications by delivering superior phase noise (-148.13 dBc/Hz at 1 MHz) and ultra-low power (2.36 mW) in 0.18 µm CMOS. Similarly, compared to [4] which achieves a -68 dBc reference spur but in a higher frequency range (5.7-6.0 GHz) with potentially higher power, [12] with phase noise of -125.8 dBc/Hz at 1 MHz but 13.4 mW power, [19] focusing on low power (7.14 mW) but with phase noise of -111.7 dBc/Hz, [13] which simulates a 2.4 GHz fractional-N PLL for WLAN without specified metrics outperforming ours, [14] emphasizing fast locking but not matching our combined metrics, and [17] with 1 µs lock time but in ADPLL architecture, the proposed design surpasses them by achieving -148.13 dBc/Hz at 1 MHz offset, 2.36 mW power consumption, and 3 µs lock time. These improvements stem from the combination of sigma-delta modulation, AVLS optimization, and efficient divider control, addressing limitations in phase noise, power, and lock speed found in prior works like [23], [24], [28]. The rest of the paper is organized as follows. Section 2 describes the multi-modulus divider, including flip-flop analysis, AVLS technique, CML blocks, and final divider design. Section 3 details the divider control bits circuit. Section 4 presents the MASH sigma-delta modulator, including single-stage and MASH-based designs. Section 5 provides simulation results, power consumption analysis, and comparisons with previous works. Finally, Section 6 concludes the paper with key findings and future directions.

II. MULTI-MODULATION DIVIDER

In the design shown in Fig. 1, a low-pass filter (LPF) has been selected, as it defines many key PLL characteristics, such as loop stability and lock speed. Filter design is crucial for the overall performance of the PLL. In this work, a third-order sigma-delta modulator is used; hence, the filter order

must also be at least three, as the power spectral density slope is +60 dBc/Hz. To compensate, the loop filter's amplitude response must have a slope of at least -60 dBc/Hz. The specific filter structure and values for R and C were obtained through MATLAB simulations and are shown in Fig. 2 [5].

The locked output frequency of the circuit is calculated using (1), where *F*out is the locked output frequency, N is the integer division factor, and *F*ref is the reference frequency [2].

$$Fout = N * Fref \quad (1)$$

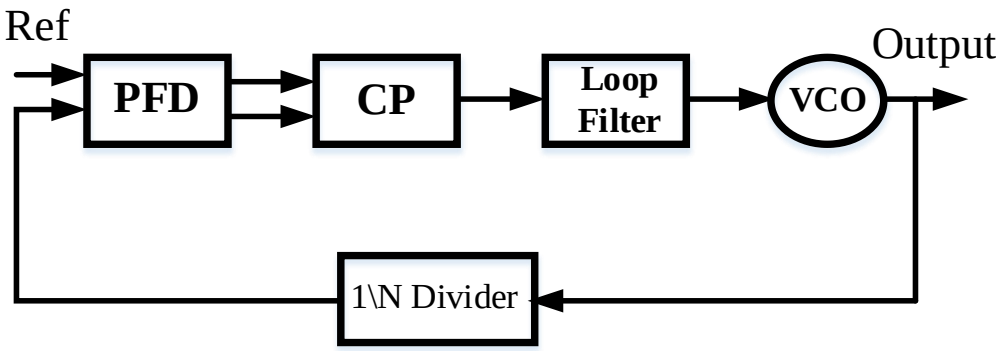

Fig. 1. Block Diagram of the Phase-Locked Loop (PLL) [24].

In the structure shown in Fig. 1, the VCO is designed to oscillate based on specified parameters within a target frequency range of 2.4 GHz to 2.5 GHz. The VCO output is fed back into the loop and divided by a specific ratio N using the Divider block. The phase of the divided signal is then compared with the reference frequency signal at the input. An error signal is generated based on the phase difference between the two signals. This phase error signal passes through the CP and LPF, which filter out unwanted high-frequency components, resulting in a smoothed signal that is then fed back to the VCO. The VCO adjusts its oscillation according to this input, and this process iterates multiple times within the loop until the phase difference between the reference signal and the signal output from the divider reaches zero. At this point, the loop is said to be "locked," which is the fundamental operating principle of a conventional integer-N frequency synthesizer.

TABLE I
Third-Order Filter Design [6]

Abbreviations	Definition	3rd order loop filter
T(s)	The loop filter's transfer function	$Z(S) = A0 * \frac{1 + S * T2}{S * A0 * (1 + S * T1) * (1 + S * T3)}$
T1	The first pole in the loop filter transfer function	$T1 \approx \frac{sec(\emptyset) - tan(\emptyset)}{wc * (1 + T31)}$
T2	The zero in the loop filter transfer function	$T2 = \frac{\gamma}{wc^2 * (T1 + T3)}$
A0	The loop filter coefficient	$A0 = \frac{KPD * KVCO}{wc^2 * N} * \sqrt{\frac{1 + wc^2 * T2^2}{(1 + wc^2 * T1^2) * (1 + wc^2 * T3^2)}}$
A1	The loop filter coefficient	*A1=A0*(T1+T3)*
A2	The loop filter coefficient	*A2=A0*T1*T3*
C1	The first capacitor in the loop filter	$C1 = \frac{A2}{T2^2} * (1 + \sqrt{1 + \frac{T2}{A2} * (T2 * A0 - A1)}$
C2	The second capacitor in the loop filter	$C2 = A0 - C1 - C3$
C3	The third capacitor in the loop filter	$C3 = \frac{-T2^2 * C1^2 + T2 * A1 * C1 - A2 * A0}{T2^2 * C1 - A2}$
R2	Resistor 2 of the 3rd order loop filter	$R2 = \frac{T2}{C2}$
R3	Capacitor 3 of the 3rd order loop filter	$R3 = \frac{A2}{C1 * C3 * T2}$
γ	Gama	1.136
T31=T3/T1	The ratio of pole 3 to pole 1	0.6

In the PLL loop design, parameters such as bandwidth (B.W.), phase margin (PM), charge pump current (ICP), and VCO gain (KVCO) are assumed to be known design values. The equations for designing a third-order filter are provided in Table I. The values of R and C required for the design, along with the schematic of the intended filter, are shown in Fig. 2.

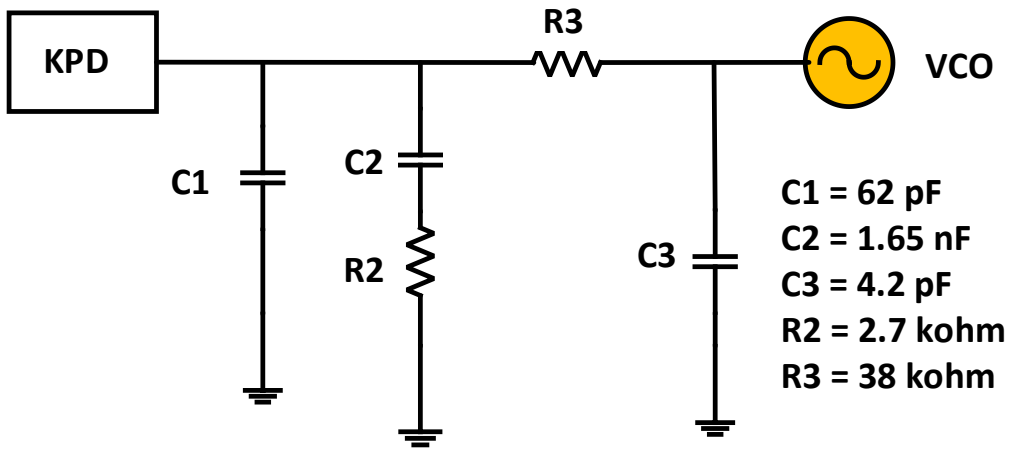

Fig. 2. Loop filter circuit and precise design values for a third-order filter [5].

The single-input single-output (SISO) Design tool in MATLAB can be utilized to calculate the resistor and capacitor values for filter design. This tool also enables the observation of loop stability and the optimal phase margin for the design, as illustrated in Fig. 3.

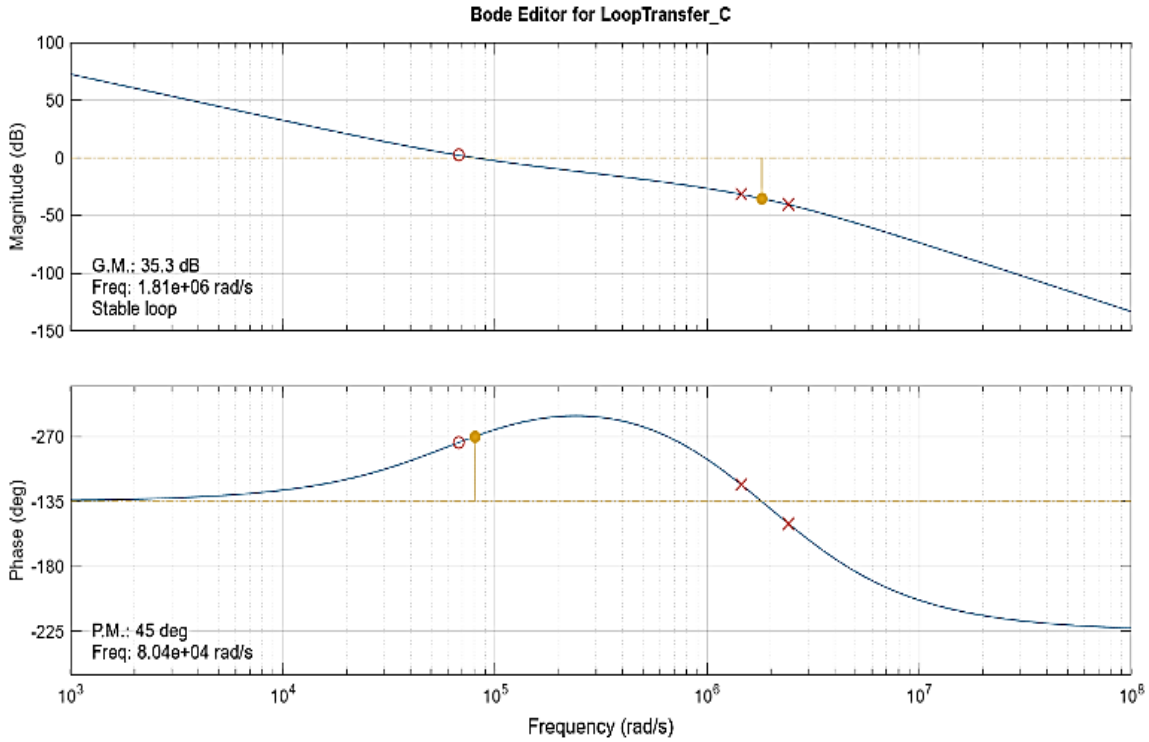

Fig. 3. Bode plot of the open-loop transfer function of the system.

The structure of this divider consists of a chain of sub-blocks, each capable of dividing by two consecutive integers. This type of divider is composed of a series of 2/3 divider blocks, with each 2/3 divider block comprising six terminals (Fin, Fout, Modin, Modout, R), as illustrated in Fig. 4 [6],[11].

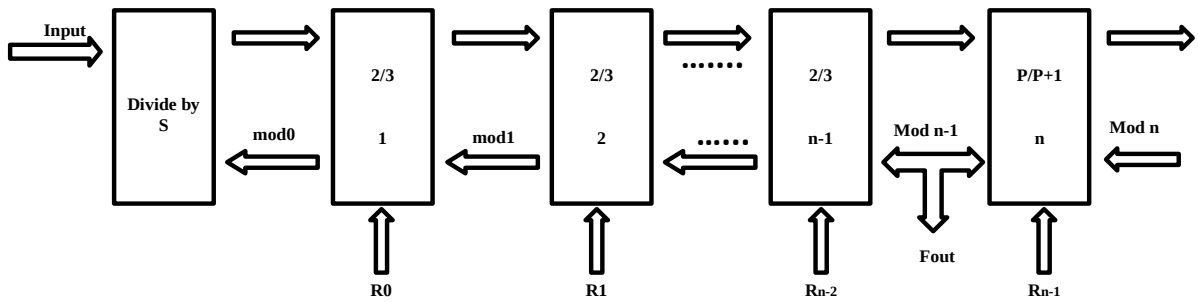

Fig. 4. Block diagram of the multi-modulus divider [6].

TABLE II.
Design of the Programmable Divider (Multi-Modulus Divider) [6]

Abbreviations	Definition	Definition
Step 1	Working frequency range	Dmin Dmax
Step 2	Sigma Delta range	[-3,4]
Step 3	New frequency range by sigma Delta	Dmin new Dmax new
Step 4	The number of dividing blocks is 2/3	$n = [\log_2(\text{Dmin new} - \text{Dmin new} + 1)$
Step 5	Determination of the last block	$\text{P}=[\frac{\text{Dmin new}}{2^{n-1}}]$
Step 6	The most ideal last block	$\text{M} = \text{P (previous)} * 2^{\text{n (previous)}}$
Step 7	The number of dividing blocks by 2/3 and determining the last final block of the MMD divider	$N = 5, P = 7, M = 7$
Step 8	General divisor	$N = 2^{n-1} * P + 2^{n-1} * R_{n-1} + 2^{n-2} * R_{n-2} + \cdots + 2^1 * R_1 + R_0$
Step 9	The dividing equation of the article	$N = 112 + 16 * R_4 + 8 * R_3 + 4 * R_2 + 2 * R_1 + R_0$

The term Fin refers to the input frequency, while Fout denotes the output frequency. The operation of the divider above is as follows: the final block of the 2/3 divider generates the Modout signal. Based on the circuit arrangement described above, this signal gradually propagates toward the beginning of the chain. Furthermore, whenever the Modin pin is active and its corresponding R pin is also active, the respective divider performs division by 3. Otherwise, if these conditions are not met, the divider performs division by 2.

In this study, a multi-modulus divider with the structure shown in Fig. 4 is utilized. Additionally, to support the frequency range of 2.4 GHz to 2.5 GHz, the divider should be capable of covering this frequency division range. Given that the reference frequency is 20 MHz, the maximum and minimum division (Dmax, Dmin) values for the divider in this study can be determined according to Table II.

Now, based on the schematic of the divider blocks presented in Fig. 4, we will examine the ideal D LATCH block (D-type flip-flop) with the minimum number of transistors, minimal power consumption, and optimal speed. This section represents the primary focus of this paper, and we will discuss it in detail in the following sections.

A. Analysis of Suitable Flip-Flop Types for Designing the Internal Blocks of the Divider

The flip-flop is a fundamental building block in digital circuits, accounting for approximately 40 to 50 percent of the total power consumption of digital systems. This has a significant impact on reducing both the delay and overall power consumption of the system. In this paper, we analyze the most efficient types of flip-flops based on various design approaches, including D-type flip-flops implemented using complementary metal-oxide-semiconductor (CMOS), clocked complementary metal-oxide-semiconductor (CCMOS), gate diffusion input multiplexer (GDI MUX), PowerPC (POWER PC), true single-phase clock (TSPC), adaptive voltage level at supply (AVLS), adaptive voltage level at ground (AVLG), self voltage level (SVL), and improved self voltage level (ISVL) architectures. We initially examine and compare several types of D-latches, then design and evaluate the corresponding flip-flops based on power and delay characteristics. Finally, we identify the optimal design for integration, which contributes to the overall optimization of the PLL system.

Based on the evaluations and comparisons of various D-latches using different techniques, according to Table III, we conclude that the TSPC (True Single-Phase Clock) logic style exhibits the best performance among the designed D-latches in terms of propagation delay, power-delay product (PDP), and transistor count. Therefore, the TSPC logic style is recommended for systems requiring high-speed operation. Additionally, the designed electronic circuit performs optimally at low voltages, which can be further optimized for power consumption by incorporating the Adaptive Voltage Level (AVL) technique for low-energy operation.

The AVL technique is divided into two approaches: AVLG and AVLS. In AVLG, the adaptive voltage level is elevated at the ground node, while in AVLS, it is raised at the supply node. Both methods help reduce the overall power consumption of the designed gate. The following sections provide an in-depth analysis and comparison of these approaches.

TABLE III.
Comparison of Design Styles [25],[26],[27]

Design Style	Power Dissipation (µW)	Propagation Delay (n sec)	PDP (µ-nJ)	Number of Transistors
CMOS	2.0	4.94	9.88	18
CCMOS	0.52	4.71	2.4492	14
GDI MUX	2.43	2.78	6.7554	12
POWER PC	0.09	30	2.7	20
TSPC	0.53	0.29	0.1537	9
AVLS*	1348	NO	NO	8
AVLG	2572.9	NO	NO	8
SVL	530.401	0.00011394	0.0604	9
ISVL*	211.28	0.00011286	0.0238	11

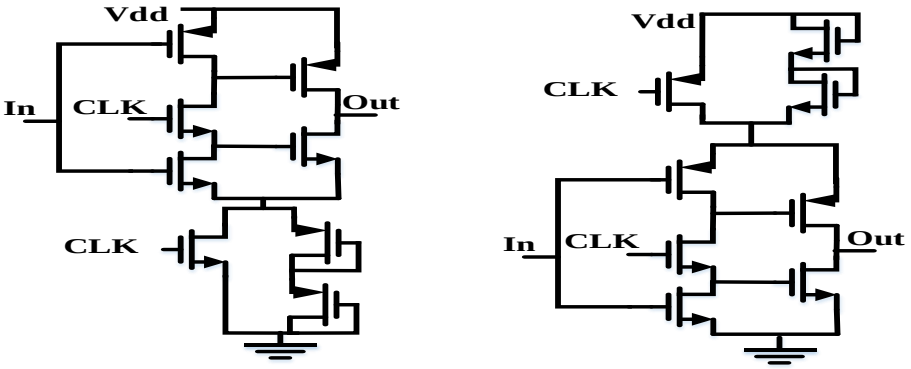

Fig. 5. D Latch circuit based on AVLG and AVLS structures [26].

TABLE IV.
Simulation Results for DFF using ISVL and AVLS Techniques

Design Style	Power Dissipation (µW)	Propagation Delay (n sec)	PDP (µ-nJ)	Number of Transistors
ISVL	36.47	0.2	7.249	**30**
AVLS	51.68	0.1	5.323	**30**

ISVL: AVLS:

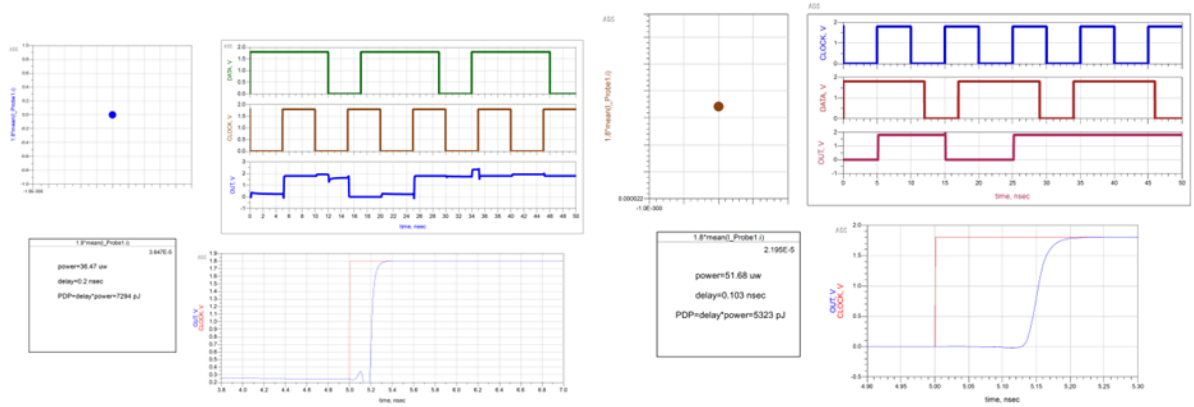

Fig. 6. Simulation Output Results for D Flip-Flop using ISVL and AVLS Techniques.

The Simulation results for the AVLG and AVLS techniques indicate that AVLS demonstrates superior performance in standby mode when comparing power consumption, delay, and PDP (Power-Delay Product) as summarized in Table IV. Based on the simulation results, AVLS provides a better PDP compared to the ISVL technique. The optimized D-latches, marked with an asterisk in Table III, are analyzed and compared based on the three key parameters presented in Table IV.

It is also important to note that while previous designs implemented D-latch structures, our design requires DFFs. Therefore, we incorporated and simulated DFF blocks in our structure. Consequently, the AVLS technique is utilized for designing 2/3 and 7/8 frequency dividers.

B. Design of 2/3 and 7/8 Divider using AVLS Technique

Based on the studies conducted on various types of DFFs, the AVLS-based DFF has proven to be the most efficient. Therefore, a D latch designed using this approach also demonstrates superior performance. Consequently, for the optimal design of the 2/3 and 7/8 divider blocks, AVLS-based DFFs and D latches can be employed to achieve the most efficient results.

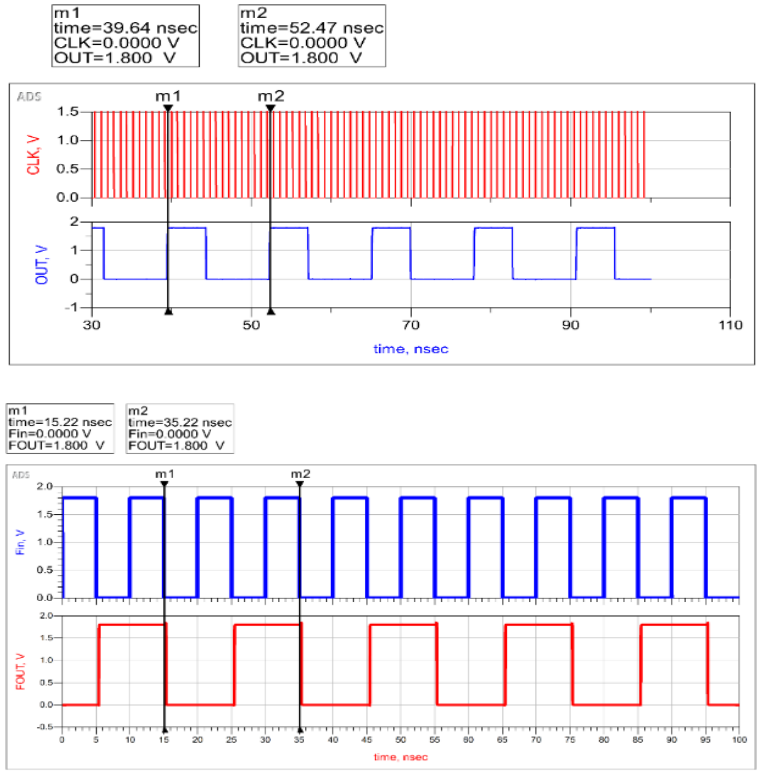

Fig. 7. Simulation Output Results for the 2/3 and 7/8 Divider Design using the AVLS Technique.

C. CML Block

The VCO output signal operates at a high frequency, so the divider circuit directly connected to it must function at this frequency. Since the overall divider is composed of smaller sub-dividers, only the first stage needs to operate at this high frequency, while subsequent stages are less critical due to the two- or three-fold frequency reduction. Designing CMOS circuits at such high frequencies is challenging. The solution is to use CML instead of CMOS logic, as CML offers both high speed and lower power consumption compared to CMOS.

Therefore, the first divider block is implemented with CML, as shown in the circuit structure in Fig. 8, with precise simulation parameters provided in Table V [28],[29].

TABLE V.
Precise Design Values for the 2/3 CML Divider Block

Design Parameters	First Block	Second Block
R	2 KOhm	4 KOhm
Ibias	400 uA	200 uA
Vswing=R*Ibias	0.8 V	0.8 V
(W/L)	2um / 0.18um	1um / 0.18um

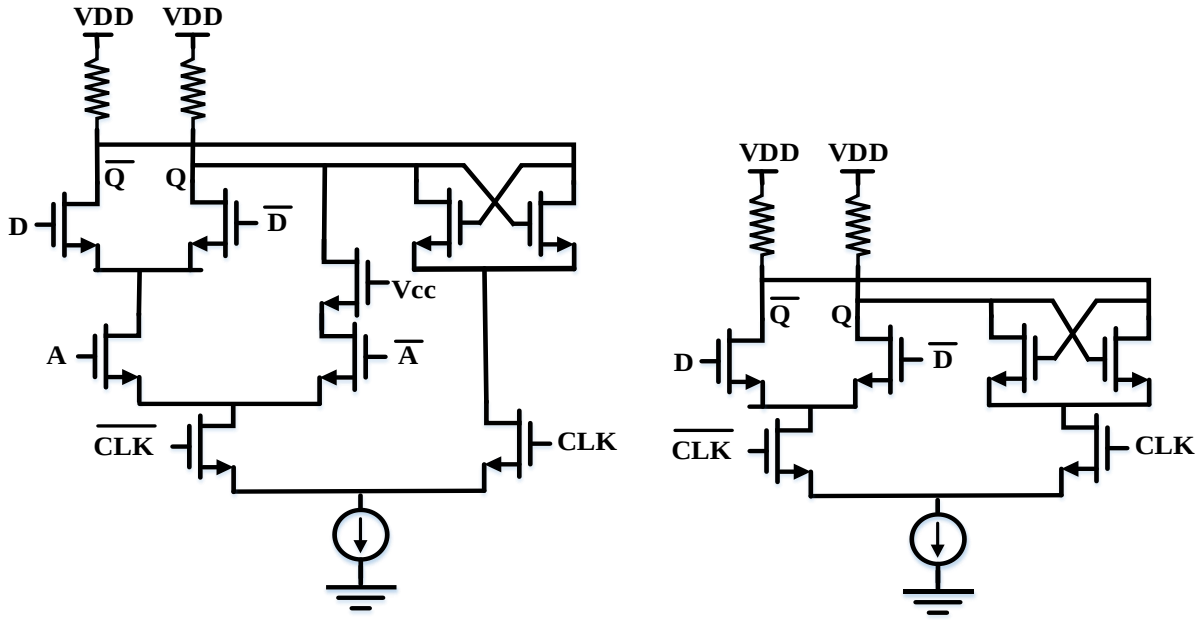

Fig. 8. Circuit Schematic of the D Latch with AND Gate and D Latch [28].

D. Design of CML to CMOS and CMOS to CML Converters

Given the voltage level differences between CML and CMOS logic, it is necessary to design a block that converts these two logic levels to enable connection to subsequent blocks and the primary divider block. This conversion block is shown in Fig. 9.

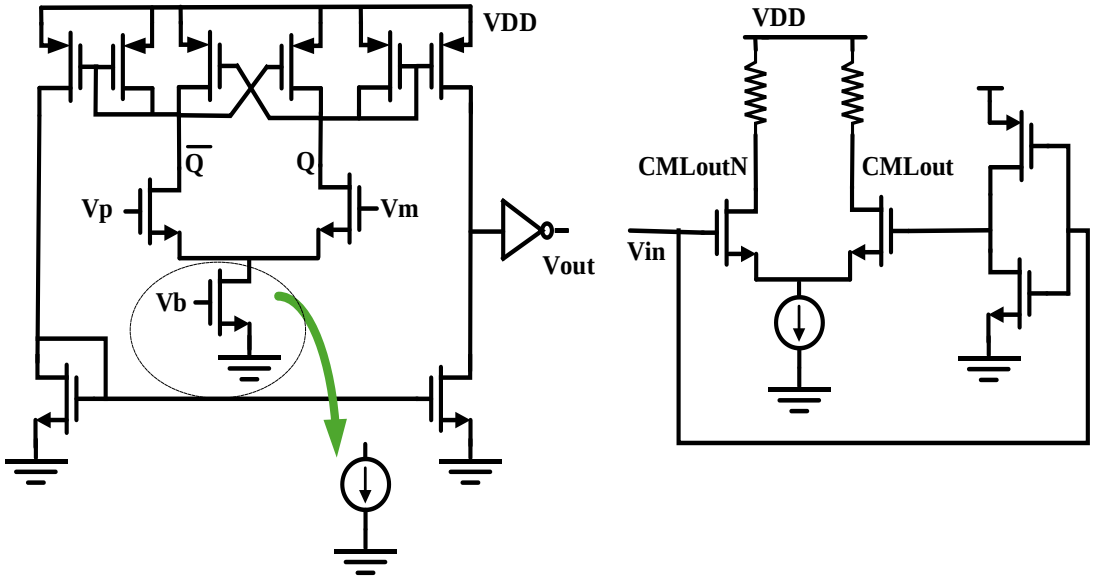

Fig. 9. CML to CMOS and CMOS to CML converter [29].

E. Final Divider Design

The overall block diagram of the divider is shown in Fig. 10. The initial blocks connected to the VCO are designed using CML logic, while the subsequent blocks utilize CMOS logic. The simulation results in ADS software are presented in Fig. 11. The values of Ri determine the division ratio via the control circuit, with the total division ratio calculated as $N = 112 + 16R4 + 8R3 + 4R2 + 2R1 + R0$. The Ri values can be either zero or one, covering a division range from 112 to 143. It is observed that when the binary representation of 122 is applied to the divider's control pins, the output, after proper analysis and simulation, also yields the division ratio of 122. By providing different values, this divider can accurately and efficiently achieve division ratios within the range of 112 to 143.

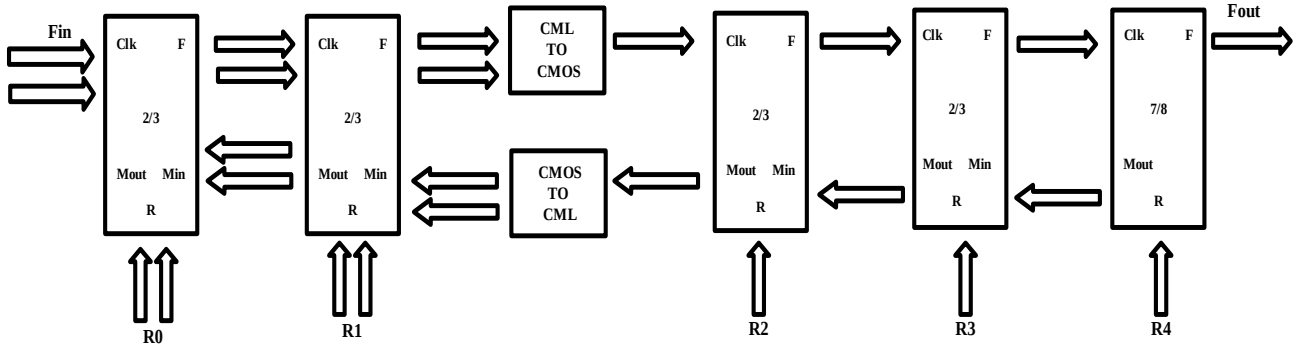

Fig. 10. Final divider design [30].

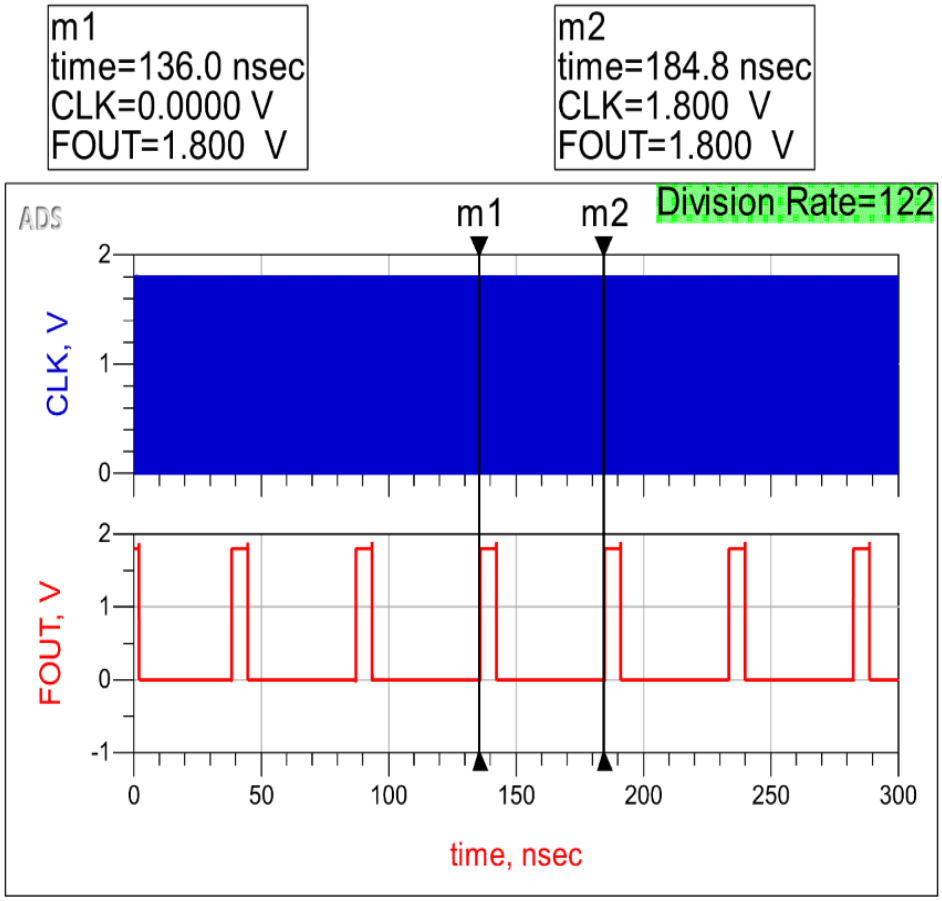

Fig. 11. Final divider output.

According to Fig. 10, the input frequency Fin is set to 2.5 GHz, and the control pins R0 to R4 are configured as 01010. Based on the simulation results, as shown in Fig. 11, the output frequency is 20.4918 MHz, indicating that the division rate is 122.

III. DIVIDER CONTROL BITS CIRCUIT

To control the pins of the final divider, the circuit shown in Fig. 12 is used. The design process begins by detailing the circuit's operation principles, with the objective of converting a decimal number to a base-5 representation. For instance, the number 122 would be converted to 01010. Initially, a decimal number is converted to a 32-bit binary format using a comparator. Then, four 8-to-3 bit converters, designed in active-high mode, are used to generate the final output. This produces a 5-bit output corresponding to the desired number, which, in this case, converts the number 122 to a 5-bit output of 01010, demonstrating the accuracy of the circuit design [31],[32].

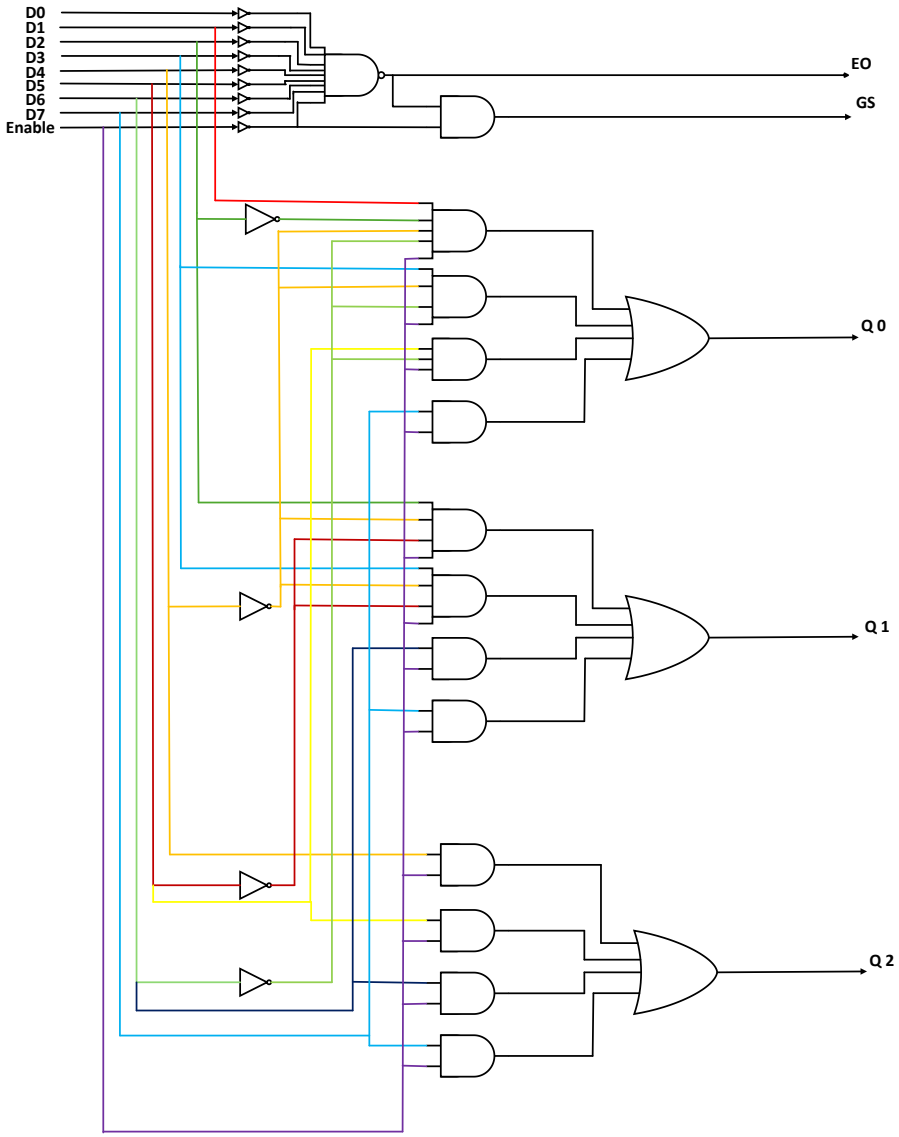

Fig. 12. Improved schematic diagram of the 8-to-3 bit converter structure [32].

Now that the design of the 8-to-3 bit converter circuit has been discussed, we can proceed to design this interface converter as shown in the schematic diagram in Fig. 12. Additionally, we can verify its functionality according to Table VI.

TABLE VI.
Truth Table for the 8-to-3bit Converter

Enable										Output				EO	GS	Decimal
	D7	D6	D5	D4	D3	D2	D1	D0		Q 2	Q 1	Q 0				Out
1	0	0	0	0	0	0	0	1		0	0	0		0	1	0
1	0	0	0	0	0	0	1	0		0	0	1		0	1	1
1	0	0	0	0	0	1	0	0		0	1	0		0	1	2
1	0	0	0	0	1	0	0	0		0	1	1		0	1	3
1	0	0	0	1	0	0	0	0		1	0	0		0	1	4
1	0	0	1	0	0	0	0	0		1	0	1		0	1	5
1	0	1	0	0	0	0	0	0		1	1	0		0	1	6
1	1	0	0	0	0	0	0	0		1	1	1		0	1	7
1																
1	0	0	0	0	0	0	0	0		0	0	0		1	0	
0	*	*	*	*	*	*	*	*		0	0	0		0	0	

The improved schematic diagram of the 32-to-5 bit converter is depicted in Fig. 13, and the output of the 32-to-5 bit converter in ADS is shown in Fig. 14.

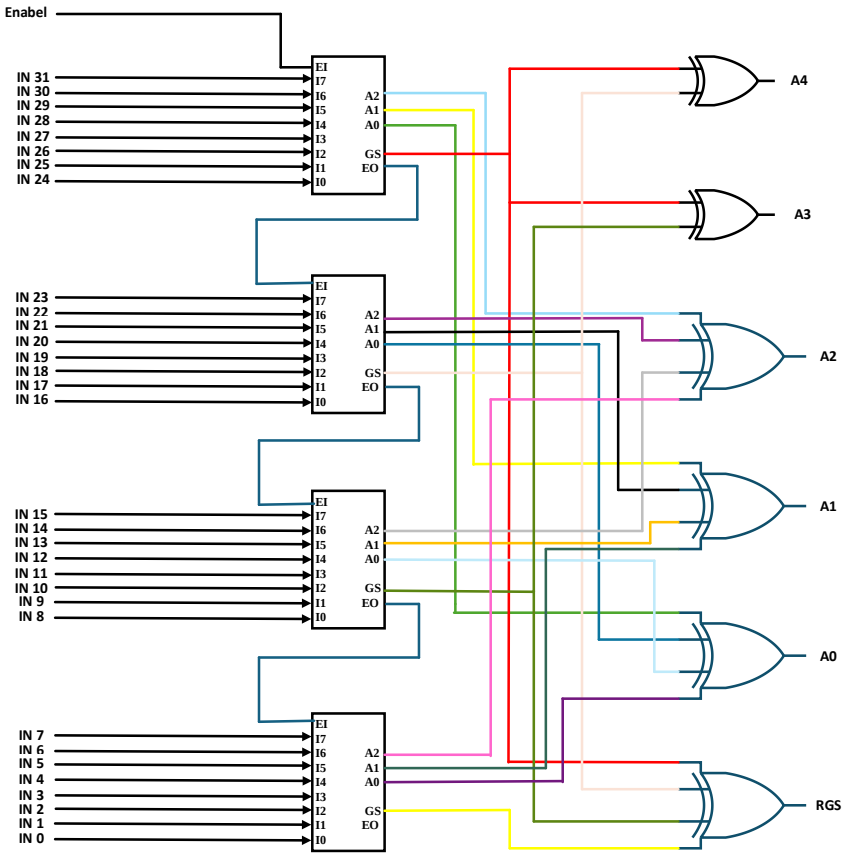

Fig. 13. Improved schematic diagram of the 32-to-5 bit converter.

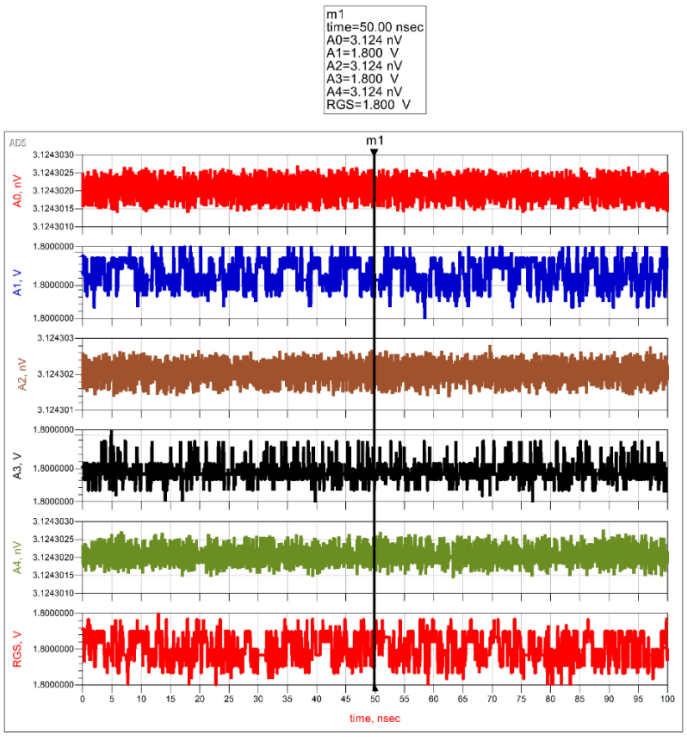

Fig. 14. Output of the 32-to-5 bit converter in ADS.

IV. MULTI-STAGE NOISE SHAPING (MASH) SIGMA-DELTA MODULATOR

An accumulator is typically required to implement a fractional-N synthesizer. However, a modulator can be used instead of a creative approach, as the modulator's output exhibits randomness, resulting in fewer unwanted tones in its power spectral density.

Thus, a first-order Delta-Sigma modulator can be used, where the operation of a first-order Sigma-Delta modulator resembles that of an accumulator, producing an overflow bit at each predefined cycle. However, this technique also has its drawbacks. Since the division occurs in the fractional domain, the generated fractional spurs propagate to the VCO, which can degrade the output. To

eliminate this effect, higher-order Sigma-Delta modulators are employed [7],[8].

The function of a Sigma-Delta modulator is to produce a random, oversampled output with noise shaping (quantization noise). In its first-order configuration, no noise is present when a DC source is used as input. However, a third-order Sigma-Delta modulator can be created by connecting two or three of these modulators in series, as shown in Fig. 15.

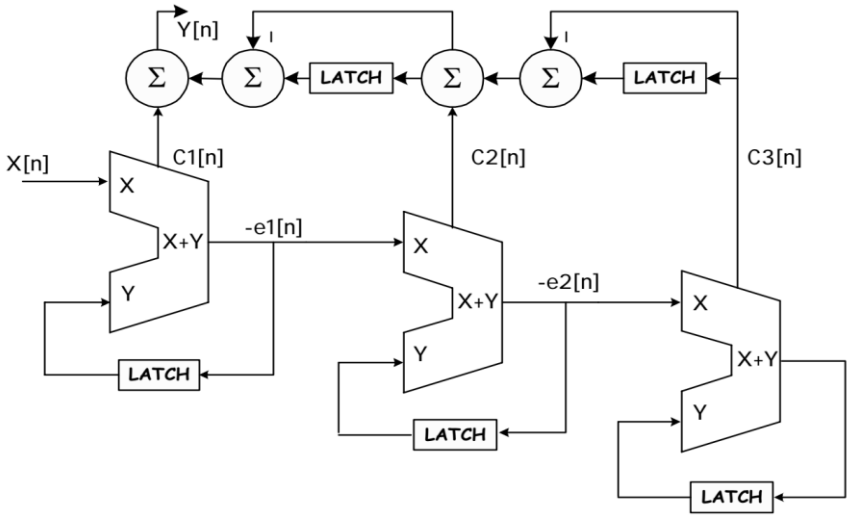

Fig. 15. Schematic of a third-order Sigma-Delta [8].

A. Single-Stage Sigma-Delta Modulator with Multiple Feedback Paths

The noise transfer function $(1-Z^{-1})^m$ can be implemented in a corresponding system using a single loop with multiple feedback paths. Although the MASH 1-1-1 method is fully stable, a single-loop SD modulator requires input amplitude reduction due to feedback loops, indicating the loop is conditionally stable. A single-loop SD modulator can produce either a single-bit or multi-bit output, whereas a MASH 1-1-1 modulator can only produce a multi-bit output.

Using a single-stage SD modulator, the number of output bits can be selected based on the quantization noise at the output and the range of division ratios within the loop. For the single-loop SD modulator shown in Fig. 16, the transfer function for an arrangement with M accumulators can be expressed as follows. It is important to note that M represents the order of the noise transfer function in the SD modulator [9].

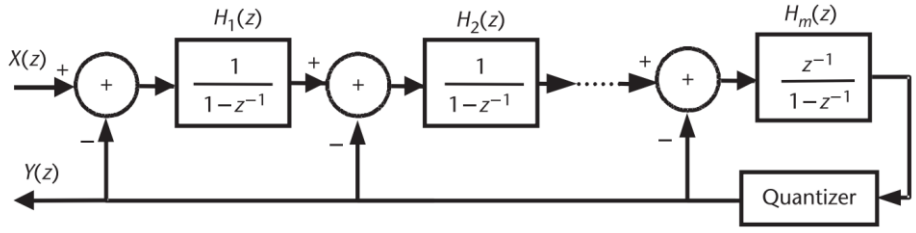

Fig. 16. Single-Stage SD Modulator with Order M [9].

$$Hi = \frac{1}{1-z^{-1}} \quad i = 1.2.3. \ \dots \ .m-1 \qquad (2)$$

$$And \quad Hm = \frac{z^{-1}}{1-z^{-1}}$$

Furthermore, the modulator output mentioned in 2 can be calculated using 3:

$$Y(z) = Hx(z)X(z) + He(z)E(z) \qquad (3)$$

In 3, the signal transfer function, represented by Hx, is calculated by 4:

$$Hx(z) = \frac{\left(\frac{1}{1-z^{-1}}\right)^{m-1}\left(\frac{z^{-1}}{1-z^{-1}}\right)}{1+\left(\frac{z^{-1}}{1-z^{-1}}\right)\sum_{i=0}^{m-1}\left(\frac{1}{1-z^{-1}}\right)^i} = z^{-1} \qquad (4)$$

Additionally, in 6, the noise transfer function, denoted as He, is calculated using 5:

$$He(z) = \frac{1}{1+\left(\frac{z^{-1}}{1-z^{-1}}\right)\sum_{i=0}^{m-1}\left(\frac{1}{1-z^{-1}}\right)^i} = (1-z^{-1})^m \qquad (5)$$

It is evident that the signal X(z) experiences only a single delay Z^{-1}, while the quantization noise is suppressed by the noise transfer function $(1-Z^{-1})^m$.

B. Design of an SD Modulator Based on MASH Structure and a Single-Loop SD Modulator with Multiple Feedback Paths

The SD structure can now be extended based on the MASH architecture, allowing it to be designed quickly for any order. Fig. 17 illustrates the circuit diagram of the improved MASH modulator.

The presented structure includes three integrator blocks and a multi-bit quantizer block (multi-bit quantizers are used instead of single-bit quantizers due to their greater stability). Additionally, the presence of gain blocks enhances the noise shaping performance throughout the entire SD modulator structure. One of the main advantages of using multi-bit quantizers is the increase in SNR, as studies have shown that for each additional quantizer bit, the SNR improves by 6 dB.

Thus, it can be stated that the Delta-Sigma modulator is an analog-to-digital converter that uses an oversampling method. In oversampling, the sampling frequency is several times higher than the Nyquist rate. Typically, high precision is achievable in these converters through noise shaping. This technique reduces noise within the band and pushes it outside the band. Various structures exist for implementation, and in this paper, the MASH 1-1-1 structure is used due to its loop stability.

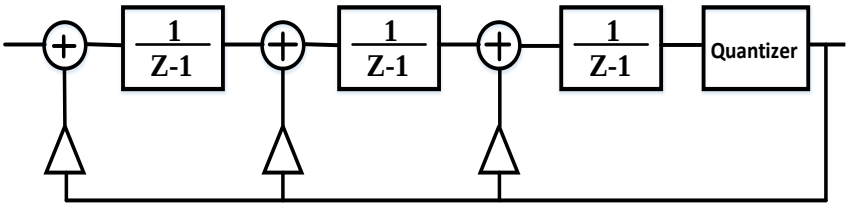

Fig. 17. Design of Sigma-Delta Modulator Based on MASH Structure [10].

The third-order sigma-delta modulator converts the decimal input signal to an 8-level output, as specified by the quantizer settings, within the range of -3 to 4 (in integer steps), as shown in Table VII.

TABLE VII.
Output Levels of the Sigma-Delta Modulator Based on Its Order

Sigma a-Delta Modulator Order	Sigma-Delta Modulator Output Levels
1	**-1,0**
2	**-1,0,1,2**
3	**-3,-2,-1,0,1,2,3,4**
4	**-7,-6,-5,-4,-3,-2,-1,0,1,2,3,4,5,6,7,8**
L	$\left(-2^{L-1}\right)+1$ **,** 2^{L-1}

V. SIMULATION RESULTS

The proposed PLL design, utilizing AVLS DFF and an intelligent control circuit, is illustrated in Figs. 18 and 19 within the ADS software, along with the corresponding simulation results. Key design parameters were selected as follows: a bandwidth of 60 kHz, a charge pump current of 250 µA, a VCO gain of 250 MHz/V, and a phase margin of 45 degrees. These parameters were chosen to optimize loop locking and to assess stability by placing the system at the edge of stability, resulting in the fastest possible locking time. Additionally, transient and envelope analysis are the two types of analyses performed in this paper. The transient analysis demonstrated an 18-fold increase in speed compared to envelope analysis, given the system specifications and simple estimation. Since both analyses yielded consistent simulation results, envelope analysis was therefore used to measure the phase noise of the loop.

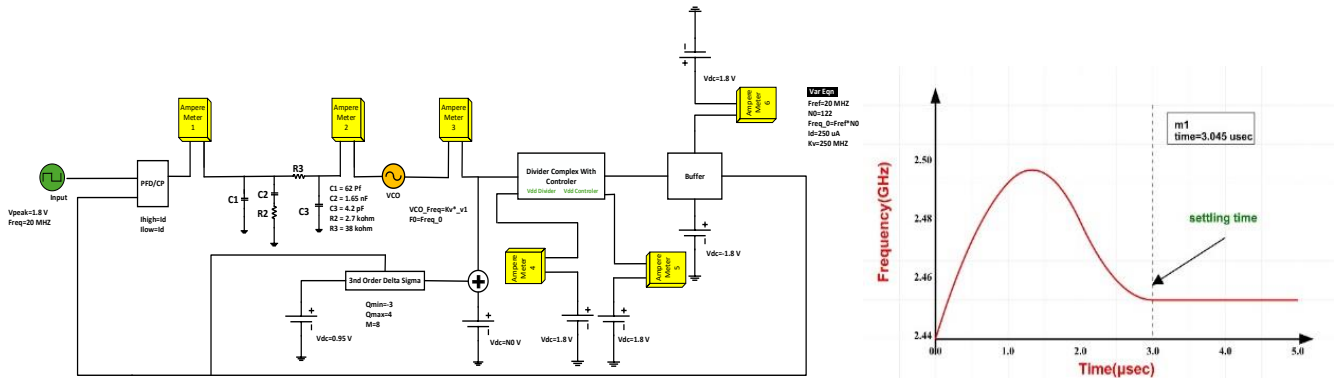

Fig. 18. Simulation of the complete PLL loop circuit in ADS software, and frequency output waveform diagram of the VCO.

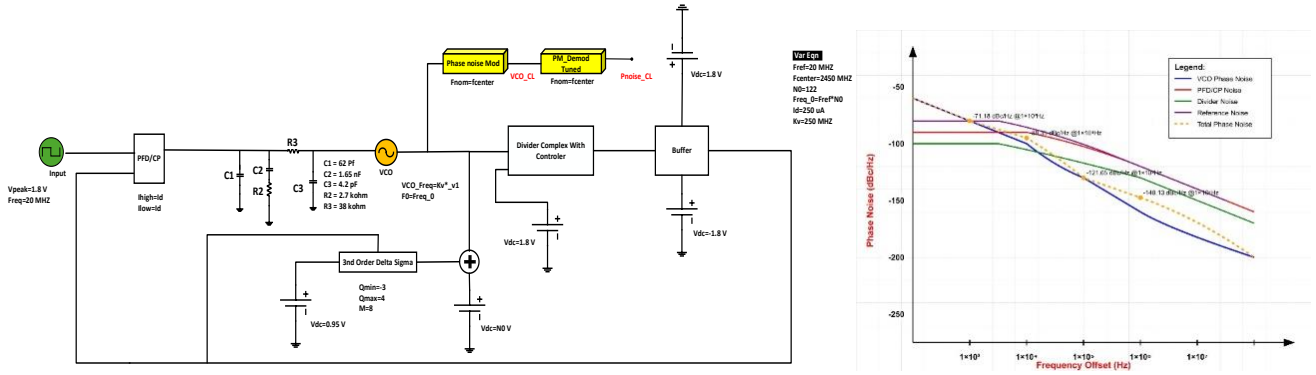

Fig. 19. The PLL loop simulation in ADS software, configured specifically for phase noise calculation.

Based on the obtained output results, the intended design achieves an optimal settling time for the entire PLL loop. Additionally, the phase noise meets expectations, demonstrating minimal susceptibility to noise.

A. Investigating the power consumption of the PLL loop and its components

According to circuit diagram number 18, the power can be calculated for each part, as shown in Table VIII.

TABLE VIII.
Table to Check the Measured Power of Each Block

N/A	A	V	Power
1	250 uA	1.8	450 uW
2	77.83 fA	1.8	140.094 fW
3	144.9 uA	1.8	260.82 uW
4	745.9 uA	1.8	1.34262 mW
5	1.155 uA	1.8	2.079 uW
6	170 uA	1.8	306 uW
Total			2.36 mW

B. Comparison of the Present Study Results to Previous Work

This study compares the proposed design to other published works, as summarized in Table IX. The table illustrates advancements in design technology, performance metrics, and operational parameters.

TABLE IX.
Comparison of the Proposed Design with Previously Published Studies

Design	**1 [9]**	**2 [33]**	**3 [13]**	**4 [14]**	**5 [15]**	**6 [34]**	**7 [16]**	**8 [12]**	**9 [17]**	**This Paper**
Technology	-	-	0.18 um	0.18 um	0.18 um	0.18 um	0.18 um	0.18 um	0.18 um	**0.18 um**
Reference Frequency	25 MHZ	20 MHZ	40 MHZ	20 MHZ	NO	NO	NO	50 MHZ	NO	**20 MHZ**
Bandwidth	200 KHZ	-	100 KHZ	60 KHZ	NO	NO	NO	100 KHZ	NO	**60 KHZ**
Frequency Range	2402 ~ 2480 MHz	200 ~ 220 MHz	2.4 GHz	2.4 ~ 2.5 GHz	1 ~ 2.3 GHz	2.5 ~ 7.3 GHz	0.01 ~ 1.5 GHz	4.5 ~ 6.1 GHz	0.7 ~1 GHz	**2.4 ~ 2.5 GHz**
Division Order	MASH 1-1	MASH 1-2	NO	NO	NO	NO	NO	NO	NO	**MASH 1-1-1**
Filter order	4	2	3	2	NO	2	NO	NO	NO	**3**
Phase Margin	50 Degree	49.9 Degree	47 Degree	NO	NO	NO	NO	NO	NO	**45 Degree**
Power	NO	NO	NO	NO	3.4 mW	13.4 mW	6.3 mW	8 mW	10.93 mW	**2.36 mW**
Phase noise dBc/Hz	-113 @ 3 MHz	-44 @210 MHz	-116 @ 2 MHz	-117 @ 1 MHz	-141 @ 1 MHz	-108.2 @ 1 MHz	-125 @ 1 MHz	-116.6 /-118.5 @ 1 MHz	-128.2 @ 100 MHz	**-148.13 @ 1 MHz**
setting time	6.5 µs	5 µs	22.03 µs	75.9 µs	NO	0.35 µs	NO	20 µs	3.5 µs	**3 µs**
Resalt	Simulated	Sim.	Sim.	Sim.	Measured	Sim.	Sim.	Meas.	Sim.	**Sim.**

This paper introduces a novel design for a Fractional-N Phase-Locked Loop (PLL) that integrates cutting-edge features such as a sigma-delta divider and AVLS D flip-flop structures, leading to significant advancements in performance. The proposed design effectively reduces circuit delay, enhances phase noise performance, and achieves an impressively fast lock time. With a settling time of 3 µs, a phase margin of 45°, and phase noise of -148.13 dBc/Hz at a 1 MHz offset, it surpasses state-of-the-art designs in terms of efficiency and precision. Furthermore, the total power consumption of only 2.36 mW demonstrates an exceptional balance between power efficiency and high performance.

The remarkable improvements achieved in this design stem from a combination of innovative elements. Intelligent control circuits play a crucial role in facilitating precise adjustments to the division ratio, thereby enhancing the system's reliability and stability. Advanced modulation and filtering techniques further optimize the loop's performance by suppressing unwanted noise and ensuring stability under varying conditions. Additionally, implementing 0.18 µm CMOS technology minimizes power consumption while enabling higher integration density, paving the way for a more compact and efficient design.

By addressing the limitations of previous designs, this work establishes a new benchmark for high-precision applications, such as GPS receivers and wireless communication networks. The proposed design not only validates its effectiveness through superior performance metrics but also highlights significant opportunities for future research and development in the field of Fractional-N PLLs. These findings underscore the potential for further innovation, setting a strong foundation for advancing PLL technologies tailored to emerging applications.

VI. CONCLUSION

This study presents a highly efficient Fractional-N PLL design, implemented using 0.18 µm CMOS technology and simulated in ADS software. The proposed PLL incorporates a sigma-delta modulator employing a MASH 1-1-1 configuration, which operates within a frequency range of 2.4 GHz to 2.5 GHz with 1 MHz channel spacing. Combining innovative techniques with meticulous optimization, the design addresses critical challenges associated with phase noise, power consumption, and lock time in modern PLL architectures.

As shown in Table IX, the proposed design achieves unprecedented phase noise performance of -148.13 dBc/Hz at 1 MHz offset, significantly surpassing prior works, which range between -44 dBc/Hz and -141 dBc/Hz. Additionally, it demonstrates the lowest power consumption among the reviewed designs, at just 2.36 mW, compared to 3.4 mW to 13.4 mW in other implementations. The system's fast lock time of 3 µs and a stable phase margin of 45° further emphasize its robustness and reliability for demanding applications. The architecture also minimizes delays and optimizes power efficiency without compromising performance, making it ideal for use in GPS receivers, wireless communication systems, and other high-precision domains.

Notably, the design exhibits exceptional phase noise characteristics across various frequency offsets: -71.18 dBc/Hz at 1 kHz, -88.35 dBc/Hz at 10 kHz, -121.65 dBc/Hz at 100 kHz, and -148.13 dBc/Hz at 1 MHz. These results reflect the effectiveness of the proposed system in achieving high precision and stability. Furthermore, the compact implementation using 0.18 µm CMOS technology highlights the potential for seamless integration in modern systems requiring low power and high efficiency.

However, the proposed design has certain limitations. It relies on simulations in ADS software and has not yet been fabricated or validated through hardware measurements, which could introduce discrepancies due to real-world factors such as process variations, temperature dependencies, or parasitic effects. The design is specifically tailored to the 2.4-2.5 GHz frequency band and may require adaptations for broader frequency ranges or different applications. Additionally, while the 0.18 µm CMOS process enables low-cost implementation, it may limit scalability and further power reductions compared to more advanced technology nodes.

Future directions for research may involve exploring the integration of machine learning algorithms to optimize the loop filter design, potentially unlocking even greater performance enhancements. By advancing the state of the art, this work establishes a robust foundation for developing next-generation Fractional-N PLLs, catering to the evolving requirements of emerging technologies and communication standards.

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