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Performance Evaluation of Reversible Universal Shift Registers in QCA Technology

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***Abstract*—The CMOS technology has been faced challenges such as high-power consumption and reduced efficiency. So, the need for alternative technologies is essential. The Quantum-dot Cellular Automata (QCA) technology is a promising solution for high-efficiency digital circuits design. The reversible circuits play crucial role in this context as they minimize energy dissipation through thermodynamically optimal computation. In addition, the shift registers have vital role in digital circuits design. They are used for storing, transferring, and converting digital data. They're also essential component in signal processing, control systems, and frequency division, enabling the creation of complex, scalable physical systems. This study focuses on the structures of reversible universal shift register implemented in QCA technology. It provides a comprehensive study on the theoretical foundations, architectures, research directions, and challenges in this field. Through systematic analysis of existing architectures and design methodologies, we evaluate key performance metrics including cell count, area efficiency, and propagation delay. Our comparative analysis demonstrates that QCA-based reversible universal shift registers achieve significant improvements over conventional CMOS implementations, offering reduced hardware complexity and enhanced energy efficiency. The results indicate potential for developing next-generation of nanoelectronics systems with superior performance characteristics. This work provides both theoretical insights and practical design guidelines that can serve as a roadmap for future researches and developments in QCA-based reversible digital circuits design.**

***Index Terms*—*Digital circuits design, Latch, QCA technology, Reversible, Shift register, Universal shift register*.**

I. INTRODUCTION

The CMOS technology has been faced limitations, particularly in terms of scalability, power consumption, and thermal issues. So, the need for alternative technologies is becoming increasingly apparent [1]. One prominent option is Quantum-dot Cellular Automata (QCA) technology, which leverages the principles of quantum mechanics and Coulombic interactions to enable the design of ultra-small, high-speed, and low-power digital circuits without the need for direct current [2], [3].

In recent years, the application of QCA in designing sequential circuits, especially universal shift registers, has garnered significant attention. These circuits play a key role in data processing and conversion [4]. Implementing these circuits in QCA technology, by reducing energy consumption and required space, paves the way for developing nano-scale digital architectures [4], [5].

Furthermore, the use of reversible logic in designing QCA circuits is thermodynamically more optimal because it prevents information loss and reduces energy dissipation [6]. For this reason, designing reversible shift registers using bidirectional gates and low-cost architectures has become an important field of QCA researches [6]–[8].

Despite these advancements, challenges such as structural complexity, the need for low temperatures for correct operation, and the lack of mass production infrastructure hinder the widespread commercialization of QCA technology. Nevertheless, advancements in nanotechnology and design tools have increased optimism for the practical application of this technology [6]–[10].

This paper examines QCA concepts and reversible logic, focusing on the design, analysis, and comparison of reversible universal shift register structures in QCA technology. The goal is to identify the advantages, limitations, and future researches direction in this emerging field.

The remainder of the paper is structured as follow. Section II provides a comprehensive background of QCA technology and structure of universal shift registers. Section III includes a comparative review of previous works. Section IV presents a comparative analysis of the findings and discussion, and finally, section V comprises the conclusion of the paper.

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II. BACKGROUNDS

A. QCA Technology

The QCA technology represents a novel approach in electronics. Instead of relying on electrical current, it uses the relative positions of electrons and Coulombic interactions to represent and transfer information. This technology makes it possible to design circuits with extremely small dimensions, very high speeds (over 1 THz), and very low power consumption [3]. Unlike CMOS technology, which faces issues like leakage current and excessive heat as transistors shrink, the QCA technology, with its different mechanism, enables higher component density and reduced energy dissipation [3]. Additionally, the QCA technology doesn't require complex physical connections and can be implemented at the nanometer scale. However, low operating temperatures and manufacturing challenges at the nano-scale are obstacles it faces [4].

In summary, the QCA technology could be an efficient and more power-efficient alternative to CMOS in future generations of digital circuits. A QCA cell is a nanoscale building block consisting of four quantum dots with two mobile electrons that, due to Coulomb repulsion, occupy opposite diagonal corners, which can represent a binary "0" or "1" based on their polarization. Fig. 1 shows the general structure of a QCA cell.

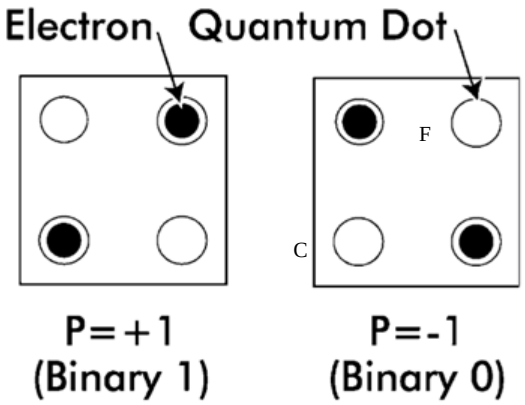


Fig. 1. General structure of a QCA cell

B. QCA Gates

In QCA technology, logic gates operate based on the electrostatic interaction between quantum dots. Unlike CMOS gates, which use electron flow, the QCA gates function by transferring state and polarization. This characteristic enables the design of circuits with very low power consumption and high speed [11].

The inverter gate is the simplest logic gate in QCA technology. It consists of several QCA cells. In this structure, the polarization of the output cell is opposite to that of the input cell. Its design is based on direct electrostatic interaction between adjacent cells, requiring no additional elements [8]. The physical structure of an inverter gate in QCA technology is shown in Fig. 2.

The buffer gate transmits an input signal without alteration. It usually consists of two consecutive inverter gates, producing an output identical to the input. This gate's main applications are maintaining signal strength over long paths and isolating different circuit sections [10].

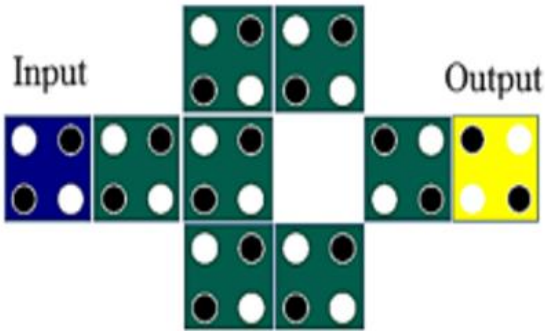


Fig. 2. Physical structure of the inverter gate in QCA technology

The majority gate is considered the beating heart of QCA logic and can implement any logical operation. This gate has three inputs and one output, with its function defined by Equation (1).

$$F = AB + BC + AC \quad (1)$$

Where F shows the output and C, B and A show the inputs.

The physical structure of this gate, shown in Fig. 3, includes five QCA cells arranged in a specific interacting configuration. This gate can implement AND and OR gates by setting one of the inputs to a fixed logic level, serving as the fundamental basis for designing more complex circuits like adders and shift registers [6].

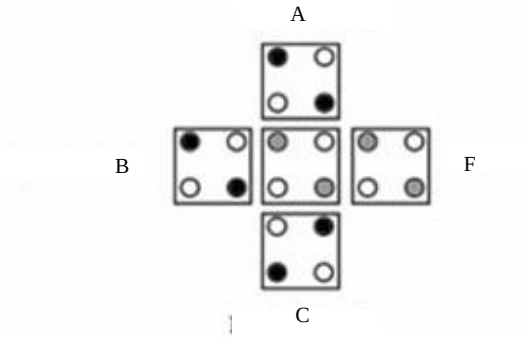


Fig. 3. Physical structure of the majority gate

The most significant challenges in the QCA gates designing include managing the four-phase clocking system, resisting environmental noise, and optimizing the balance between area and delay. Nevertheless, these gates hold high potential for use in designing arithmetic-logic units, memories, and advanced shift registers, serving as a foundation for a new generation of low-power computing systems [12].

C. Universal Shift Register

The universal shift register is a widely used and flexible sequential circuit in digital circuits design that provides all functional modes of shift registers. This shift register can receive data in series or parallel and deliver it to the output. It can also shift information to the left or right and retain previous data [6]. These features make it a key component in data processing, buffering, serial-to-parallel and parallel-to-serial conversion, and control and computational systems [4].

In traditional implementations with CMOS technology, universal shift registers are designed using D-flip-flops or latches and control circuits. However, due to scalability and power consumption limitations in CMOS, researchers have turned their attention to novel technologies such as QCA technology [5].

In the QCA technology, due to its nanometer dimensions and unique operating mechanism, implementing universal shift registers with high density and very low power consumption becomes possible. Furthermore, using reversible logic in these designs can reduce energy dissipation, which is highly significant for futuristic architectures such as quantum computing and ultra-low-power systems [9][13]. Fig. 4 shows the schematic of a reversible universal shift register.

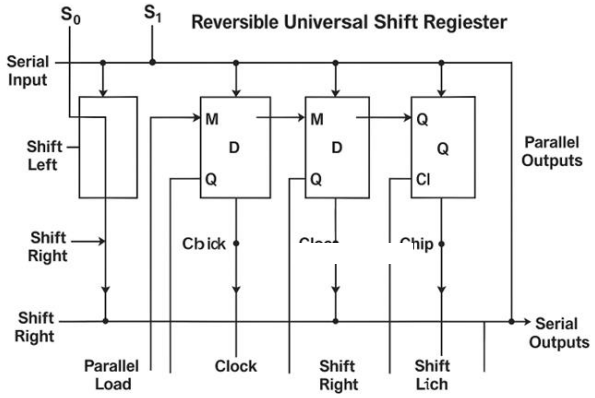


Fig. 4. Block diagram of a reversible universal shift register [9]

The universal shift register is found in many digital applications, and its combination with QCA technology, especially in the form of reversible designs, promises a new generation of low-power, fast, and compact circuits in nanoelectronics [14]–[16].

III. RELATED WORKS

Prakash et al. [7] presented a novel reversible shift register circuit. The physical structure of this new shift register, introduced in [7], is shown in Fig. 5.

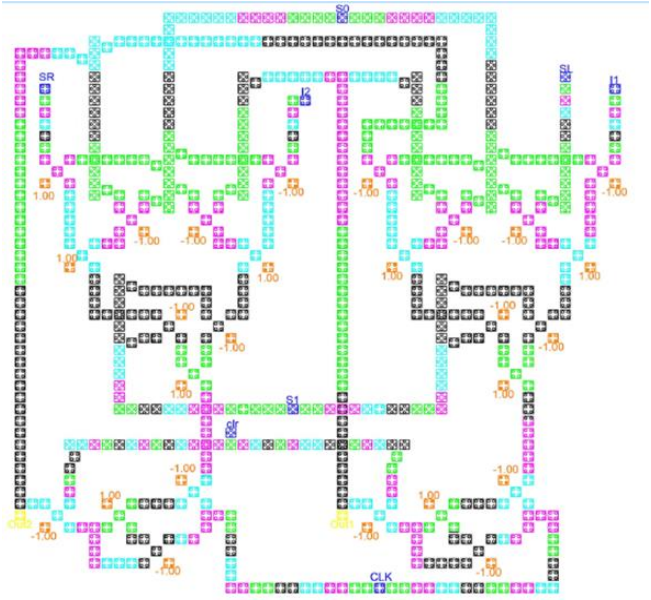


Fig. 5. The physical structure of the QCA universal 2-bit shift register presented in [7].

This 2-bit universal shift register was developed in QCA technology, comprising a 4x1 multiplexer and D flip-flops, and constructed using reversible majority gates. This shift register is capable of performing left shift, right shift, and parallel load operations.

Rupali Singh and Pankaj Singh [10] have presented a new physical structure for a shift register in QCA technology by employing a novel Fredkin gate structure. The physical design of the proposed QCA shift registers in [10] is shown in Fig. 6.

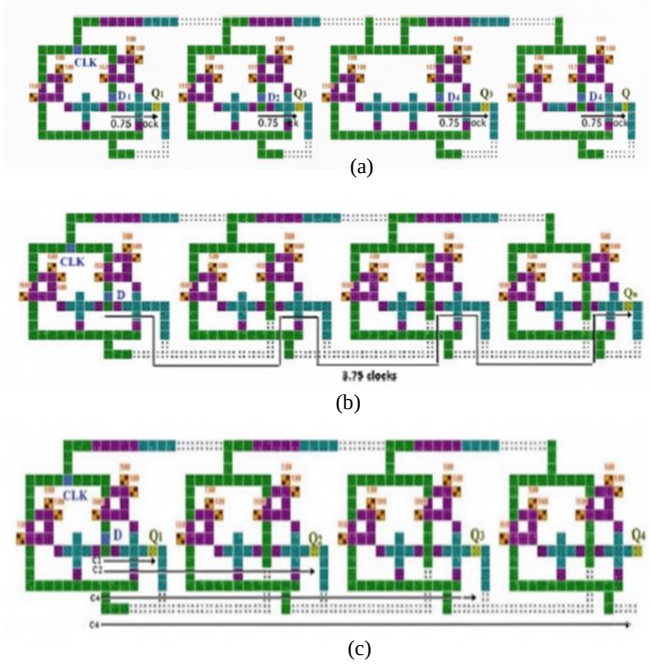
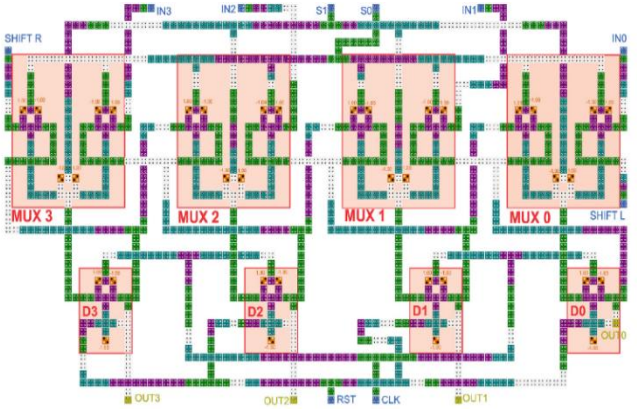


Fig. 6. The physical structure of the shift registers presented in [10] a) PIPO b) SISO c) SIPO.

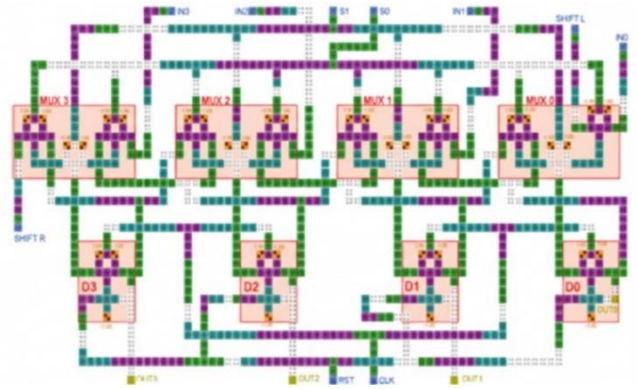
In [10], the authors designed 4-bit reversible SISO, SIPO, and PIPO shift registers based on QCA technology. Each of these is composed of four reversible gates and occupies an area of 0.4 μm². The SISO shift register has the longest delay, with 3.75 clock cycles for the final output, whereas the PIPO shift register has the shortest delay at 0.75 clock cycles. The delay of the SIPO shift register varies for each output, ranging from 0.75 to 3.75 clock cycles. Each shift register is made up of four D flip-flops and includes approximately 1348 QCA cells.

Roushan and Gholami [8] introduced new universal shift registers in QCA technology that have reset capabilities. The physical structures of the proposed shift registers in [8] are depicted in Fig. 7.

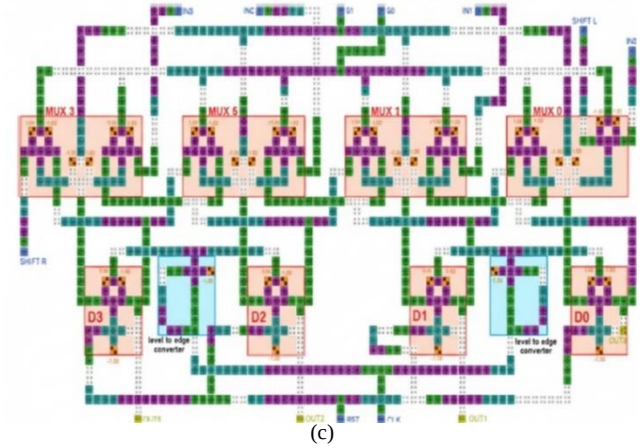
In this implementation, the core blocks, such as D-flip-flops and 2x1 and 4x1 multiplexers, are designed and interconnected to create comprehensive universal shift register functionality. The authors present three different design variants with progressive optimization. The initial design, Fig. 7 (a), covers an area of 1.57 μm² with 1220 cells and maintains a constant final circuit delay of 3 clock cycles. The optimized level-triggered version, Fig. 7 (b), achieves better performance with 1057 cells occupying 1.27 μm² area while preserving the same 3 clock cycles delay. The edge-triggered variant, Fig. 7 (c), incorporates rising edge sensitivity with 1085 cells and 1.27 μm² area, demonstrating the feasibility of adding advanced clocking features without significant area penalty. The results indicate that positioning inputs and outputs outside the main layout simplifies routing and contributes to overall design optimization across all three variants.



(a)



(b)



(c)

Fig. 7. The physical structure of the shift registers presented in [8] a) using D-latches with reset ability b) the improved model and c) the proposed model with rising edge clock.

Gholami [3] has proposed a novel serial communication system using a PISO shift register and a SISO shift register. The proposed serial communication is illustrated in Fig. 8.

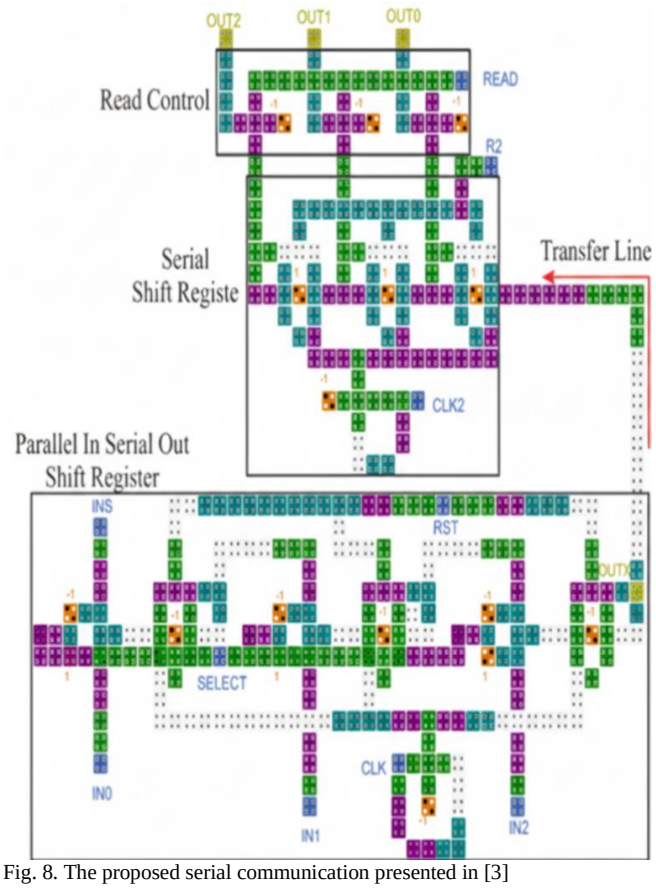


Fig. 8. The proposed serial communication presented in [3]

To construct the edge-triggered SISO shift register, a converter was used in the clock input path. Simulation of the reversible SISO shift register demonstrates that data is sequentially stored in the flip-flops and appears at the output. The proposed PISO shift register was implemented in three layers, occupying an area of 0.3 μm² with 257 cells, and an edge detection converter was utilized on the clock inputs of the flip-flops. Additionally, the proposed serial communication in [3], implemented with a PISO shift register and a SISO shift register, allows data to be sequentially transmitted to the SISO shift register's logic by activating the SELECT input in the PISO. The transfer line represents the data communication pathway between PISO and SISO shift registers, enabling sequential data transmission through controlled activation of the SELECT input signal.

IV. COMPARISON AND DISCUSSION

This section compares and analyzes various reversible shift register designs based on QCA technology that are introduced previously. Table I summarizes the main characteristics of these designs.

TABLE I
Comparative Summary of Previous Studies

Reference	Cell count	Area (μm²)	LAT	CLK	Crossover	ALC	Features	Limitations
[7]	648	1.02	4	16	coplanar	4.08	2-bit universal shift register with reversible majority gates; improved operational density; support for multiple shift modes	Significant propagation delay affecting high-speed applications
[10]	420	0.4	3.75	15	coplanar	1.5	Novel Fredkin gate implementation; 4-bit SISO register with reversible D-latches; single layer design;	complexity in combinational logic implementation
[8]	Fig.7(a): 1220, Fig.7(b): 1057, Fig.7(c): 1085	Fig.7(a): 1.57, Fig. 7(b): 1.27, Fig. 7(c): 1.27	3	12	coplanar	Fig.7(a): 4.71, Fig. 7(b): 3.81, Fig. 7(c): 3.81	Reset capability integration; consistent delay performance; optimized routing design; robust control mechanisms	Increased wiring complexity; practical implementation challenges in nanoscale fabrication
[3]	SISO: 111 PISO: 257	SISO: 0.1 PISO: 0.3	3.25	13	SISO: single layer, PISO: multilayer	SISO: 0.325, PISO: 0.975	Ultra-low cell count for SISO; exceptional area efficiency; innovative PISO multilayer design; serial communication capability	PISO multilayer design complexity; increased manufacturing costs

In this table LAT and CLK indicate the total clock cycles and total clock phases, respectively. In addition, the ALC is computed as follows.

$$ALC = Area \times Latency \quad (2)$$

The comparative analysis reveals that current research demonstrates focused efforts on optimizing fundamental performance parameters. The results indicate significant variations in design approaches, with cell counts ranging from 111 to 1220 cells and area efficiency varying from 0.1 μm² to 1.57 μm². Clock cycle requirements vary from 3 to 4 cycles across different designs. The ALC values demonstrate that the SISO shift registers in [3] achieves the best area-latency trade-off at 0.325, while the designed circuit in [8] shows the highest ALC value of 4.71. Note that the number of input bits for different designs may not be equal.

The evaluation demonstrates that multilayer designs offer superior area efficiency, but introduce manufacturing complexity and potential reliability concerns. Coplanar designs provide manufacturing simplicity, but typically require larger areas and may suffer from wiring congestion. The crossover implementation choice significantly impacts both area and delay.

The analysis identifies several critical challenges for practical implementation including fault tolerance mechanisms, clock signal stability, and thermal noise immunity. Manufacturing precision requirements for multilayer designs and long-term reliability considerations under varying environmental conditions present additional hurdles for commercial viability. The standardized comparison reveals that achieving optimal performance requires careful consideration of application-specific requirements and manufacturing constraints.

V. CONCLUSION

This paper explores and compares various designs for implementing reversible shift registers in QCA technology. Research primarily focuses on reducing QCA cell count, area, delay, and ALC. Designing efficient universal shift registers is possible using reversible latches and innovative logic gates.

The main challenge lies in achieving an optimal balance between area, delay, and quantum cost. Furthermore, more attention is needed for investigating multilayer structures, developing algorithms and CAD tools, and analyzing practical implementations. Integrating QCA with novel technologies like carbon nanotubes can enhance the efficiency of these circuits.

The results indicate that QCA technology holds significant potential for implementing high-speed, low-power, and scalable reversible shift registers playing a crucial role in the next generation of processing systems. In addition, the universal shift registers will serve as critical components in next-generation processing and memory systems. The convergence of reversible logic principles with QCA technology foundations can establish a clear pathway toward quantum computing architectures and ultra-efficient nanoelectronics systems.

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