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Modeling and Simulation of Pc-ZnO TFTs using AI/ML Techniques

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***Abstract* — This work develops a machine learning-based model to accurately predict the electrical characteristics of Polycrystalline Zinc Oxide Thin-Film Transistors (Pc-ZnO TFTs). A Random Forest regression model is trained using combined data from multiple drain current versus gate voltage ($I_D - V_{gs}$) and drain current versus drain voltage ($I_D - V_{ds}$) s1weeps, capturing the complex nonlinear behavior of the device. The model achieves high accuracy, with prediction errors below 1% in most cases, and is validated through comparisons with TCAD-simulated I–V characteristics. The full current–voltage (I–V) curves in forward voltage sweeps are predicted well, with high R-squared values of 0.9938 for $I_D - V_{gs}$ and 0.9953 for $I_D - V_{ds}$. This method can replace traditional compact models, which often struggle to capture the variability of Pc-ZnO TFTs, by providing a fast, reliable, and scalable modeling approach. Moreover, the model can be integrated into circuit simulators such as SPICE via Verilog for device- and circuit-level simulations. This study highlights the potential of machine learning techniques to advance compact modeling and support the development of next-generation electronic displays and flexible devices.**

***Index Terms*— Pc-ZnO TFTs, Characterization, Machine Learning (ML), Random Forest Regression.**

I. INTRODUCTION

Thin-film transistors (TFTs) are at the heart of today's flat-panel displays, driven by the unique advantages of oxide semiconductors such as zinc oxide (ZnO) [1]. These materials draw attention because they combine low-cost fabrication with higher electron mobility and optical transparency compared to conventional a-Si TFTs [2]. Researchers are especially interested in polycrystalline ZnO (Pc-ZnO) and GaInZnO channels for next-generation applications, such as transparent circuits and flexible displays [3]. TFTs are highly sensitive to stresses, including bias, temperature shifts, light exposure, and mechanical strain, all of which can reduce their long-term performance [4]. Among these factors, the role of temperature in Pc-ZnO TFTs is not yet well understood, making it difficult to fully explain their conduction behavior and reliability under real-world conditions [4].

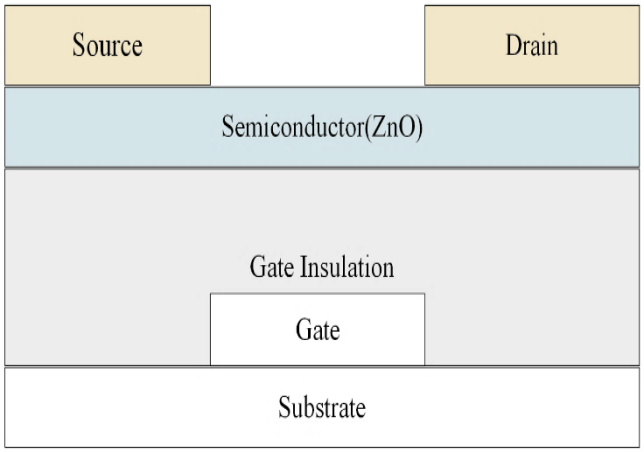

Fig. 1. Pc-ZnO TFTs structure

Pc-ZnO can exist in two crystal forms—hexagonal wurtzite and cubic zincblende—with the wurtzite phase most commonly found in thin films due to its higher stability. It typically behaves as an n-type semiconductor with a bandgap of approximately 3.37 eV, offering chemical stability, optical transparency, and compatibility with low-temperature processing, which makes it well-suited for flexible and large-area electronics [5-20]. However, modeling Pc-ZnO TFTs is not straightforward because of their nonlinear behavior, dependence on gate and drain bias, and variability introduced during fabrication. Conventional compact models often struggle to capture $I_D - V_{gs}$ and $I_D - V_{ds}$ behavior across the full range of operation and rely on complex parameter extraction, which limits their scalability and practicality [5].

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Modeling Pc-ZnO TFTs presents significant challenges due to material disorder, grain boundaries, trap states, and bias-stress instabilities, which can cause mobility degradation and threshold voltage shifts [3,5]. Additionally, nonlinear I–V behaviour, data scarcity, and device variability make accurate prediction difficult. Traditional compact models often fail to capture the variability of Pc-ZnO TFTs [3-7], whereas ML-based approaches, including Random Forest regression, have been shown to provide accurate and scalable predictions [2-11]. Physics-based models are often too slow for circuit-level use [3], while purely data-driven ML approaches risk overfitting, poor generalization to unseen biasing or stress conditions, and limited physical interpretability [2]. Current research is also limited by restricted and noisy datasets, the lack of hybrid physics-informed architectures, weak coverage of small-signal and dynamic reliability effects, and limited transferability across geometries, processes, and environments [2-5]. These gaps highlight the need for scalable, interpretable, and hybrid AI/ML frameworks that couple physical mechanisms with data-driven learning to achieve accurate, robust, and generalizable Pc-ZnO TFT models [2-3].

To overcome these challenges, this work introduces a machine learning (ML)-driven method that employs Random Forest regression to build a unified predictive model for Pc-ZnO TFTs [5-6]. By training on datasets containing multiple $Id - Vgs$ and $Id - Vds$ sweeps, the model can capture the complex nonlinear behaviour of the devices while delivering accurate predictions suitable for integration into circuit simulators such as SPICE [7-10]. This approach helps close the research gap by providing a fast, adaptable, and reliable modeling framework that supports both device-level optimization and system-level analysis, creating new opportunities for advances in display and flexible electronics [7,10].

Several recent studies have demonstrated the effectiveness of machine learning (ML) techniques for predicting transistor characteristics. Kumar et al. [2] applied ML to optimize and accurately predict performance parameters of stacked nanosheet transistors. Liu et al. [8] introduced Random Forest as a robust algorithm for regression tasks, highlighting its low computational cost and resilience to noisy data. Ozer et al. [10] developed a hardwired ML engine using submicron metal-oxide TFTs on flexible substrates, demonstrating hardware-level integration of ML for device modeling. Butola et al. [11] presented a comprehensive ML-based framework for gate-all-around nanosheet transistors, emphasizing accuracy in device and circuit modeling. Choi et al. [12] applied ML for automatic prediction of MOSFET threshold voltage, while Singh et al. [14] combined ML with statistical variation analysis for ferroelectric transistors (FE-MOSFETs).

More recently, Rajan et al. [18] used hybrid ML models to predict reconfigurable FET characteristics with limited datasets, Chankla et al. [19] demonstrated accurate I_d–V_g modeling in SiC MOSFETs using neural networks with small training data, and Ghoshhajra et al. [20] evaluated junction less FinFET performance using TCAD-enabled deep learning. Collectively, these works highlight the growing role of ML in transistor modeling, emphasizing accuracy, scalability, and integration with physical and circuit-level constraints, which motivates the application of Random Forest regression for Pc-ZnO TFTs in this study. Similarly, Khani et al. [21] demonstrated the use of machine learning to model Fano resonance–based plasmonic refractive index sensors, further underscoring the versatility of ML in accurately capturing nonlinear physical phenomena across semiconductor and photonic devices

A. Problem statement

Modeling thin-film transistors (TFTs), particularly those based on polycrystalline zinc oxide (Pc-ZnO TFTs), is a challenging task due to their highly nonlinear behaviour and sensitivity to bias conditions. Traditional compact models often fall short in accurately capturing these effects, especially under varying gate and drain voltages. These models also require complex parameter extraction, which reduces flexibility and scalability. To address these limitations, our work explores a machine learning-based approach using Random Forest regression to develop a more accurate and reliable model. The goal is to create a compact model that not only fits the data well but can also be integrated into standard circuit simulators such as SPICE for real-world applications.

Machine learning (ML) is poised to play a key role in advancing predictive capabilities in semiconductor device compact modeling. One major advantage of ML-based compact modeling is its ability to capture complex relationships and patterns in large datasets [7]. This paper proposes a unified machine learning-based framework for accurately predicting the drain current characteristics of Pc-ZnO TFTs using Random Forest regression [8].

By training on a dataset comprising multiple $Id - Vgs$ and $Id - Vds$ sweeps, the model captures the intricate device behavior with high accuracy [5,9]. The approach also allows future integration into circuit simulators through Verilog, facilitating both device- and system-level analysis [10]. Our work demonstrates that AI/ML techniques can significantly accelerate the development of compact models for oxide TFT technologies [7,10], opening new pathways in display and flexible electronics [4,11–12].

II. Device description and simulation methodology

A. Device description

TFT operation is based on the field-effect transistor (FET) principle, where the gate voltage controls the electric field in the semiconductor channel [1,5]. This field influences charge carriers, altering the channel conductivity and thus the current between the source and drain [1,2]. For small drain-source voltages (Vds), the drain current (Id) varies linearly with Vds, and the channel behaves like a resistor [4,8].

$$\mathbf{I_d = G_d . V_{ds}} \quad (1)$$

Where G_D is defined as the drain conductance. The channel conductance is given as,

$$\mathbf{G_o = \frac{w}{L\mu|Q|}} \quad (2)$$

Where W is the transistor channel width and L is the transistor channel length, μ is the field-effect mobility of the charge carriers in the channel, Q is the magnitude of the sheet density of the accumulated layer charge, and is a function of the gate-source voltage (V_{gs}) and the capacitance per unit area of the gate insulator C_i [2, 11]. In the absence of traps, the accumulated layer charge is given as a product of,

$$|Q| = C_i(V_{gs-}V_{th}) \quad (3)$$

Where V_{th} is the threshold voltage and C_i is the capacitance per unit area, given by

$$C_i = \frac{\varepsilon.\varepsilon_o}{t_i} \quad (4)$$

The performance of a TFT is typically characterized by its drain current, field-effect mobility, and threshold voltage [1, 11]. The drain current is the current flowing between the source and drain electrodes when a voltage is applied to the gate electrode, and is a measure of the transistor's overall current-carrying capacity [3, 5]. The field-effect mobility is a measure of the speed at which charge carriers move through the channel in response to the electric field created by the gate voltage [1, 8, 12]. The threshold voltage is the voltage required to turn the transistor on, and it is influenced by the properties of the gate dielectric and the semiconductor material [2, 11].

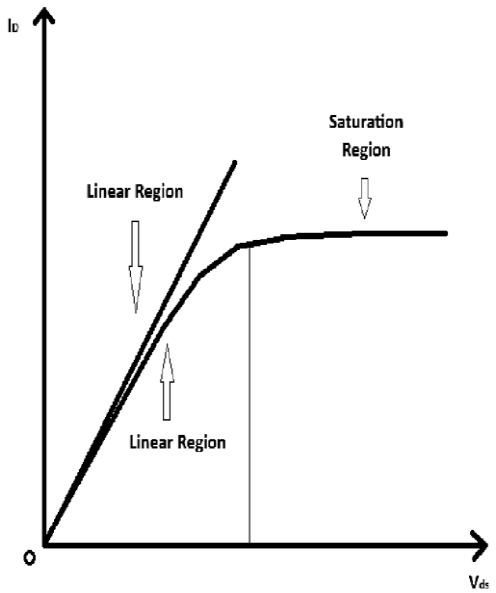

Fig. 2. Transfer characteristics $I_d = f(V_{ds})$ of the Pc-ZnO TFTs.

In the linear region of transistor operation, when $V_{ds} < V_{gs} - V_{th}$ (meaning when the bias voltage applied to the gate minus the threshold voltage is larger than the voltage applied between source and drain), the following expression is used to describe the drain current Id [2, 3, 8].

$$I_{ds} = \frac{w\mu C_i}{2L}[2((V_{gs-}V_{th})V_{ds} - {V_{ds}}^2)] \quad (5)$$

For small VDS ≪ (VGS − Vth), the TFT operates in the linear region, where the drain current increases linearly with gate voltage. The slope of the I–V curve is determined by device parameters, such as mobility and channel dimensions [2, 3].

$$I_{ds} = \frac{w\mu C_i}{2L}[((V_{gs-}V_{th})V_{ds})] \quad (6)$$

It is important to note that the linear region of operation is limited by the maximum drain voltage that the TFT can withstand without breakdown, typically around 15–30 V for Pc-ZnO TFTs [3, 5]. Beyond this voltage, the TFT enters the saturation region, where the drain current levels off and becomes independent of the drain voltage [2, 11]. For a large drain-to-source voltage VDS > (VGS − Vth) and VGS > Vth, the transistor is biased in the saturation region of operation. In this case, because of the high V_{DS} voltage, V_{GS} is reduced at the drain end of the channel, and therefore the channel depth decreases to almost zero, so-called pinch off [2, 3, 8].

In this region, the TFT is fully on, and the drain current is limited by channel resistance, electron mobility, and the electric field [2]. Increasing Vgs has little effect, and the drain current saturates, varying roughly with the square of the gate voltage [2, 3, 11].

The saturation drain current can be obtained by replacing $V_{ds} = V_{gs} - V_{th.}$ This is shown in the following expression:

$$I_{ds} = \frac{w\mu C_i}{2L}[(V_{gs-}V_{th})^2] \quad (7)$$

By controlling the parameters in the drain current equation, such as gate voltage, channel length, and width, and effective carrier mobility, the saturation region of a TFT can be engineered to achieve desired performance characteristics, such as high on-state current, low off-state leakage, and good linearity. Understanding and optimizing the saturation region behavior is essential for designing TFT-based devices [12-20].

TABLE I

Model Parameters for Pc-ZnO TFTs

Parameter	Value
Electron affinity	4.29 eV
Dielectric constant	8.12
Electron mobility	40 $cm^2/V{\cdot}s$
Hole mobility	1.5 $cm^2/V{\cdot}s$
Effective conduction band states	4.3×10^{18} cm^{-3}
Effective valence band states	4.3×10^{18} cm^{-3}
Energy gap at 300K	3.4 eV
Density of acceptor-like tail states	$3.6\times10^{21} cm^{-3}{\cdot}eV^{-1}$
Density of donor-like tail states	4×10^{19} $cm^{-3}{\cdot}eV^{-1}$
Capture a cross-section of electron and hole states	4.0×10^{-15} cm^2
Characteristic decay energy (acceptor-like tail states)	0.12 eV
Characteristic decay energy (donor-like tail states)	0.1 eV

B. Description of numerical simulation framework

TFT performance is evaluated via $I_d - V_{ds}$ and $I_d - V_{gs}$ curves. The $I_d - V_{ds}$ curve, obtained by varying Vds at constant Vgs, shows linear and saturation regions for extracting parameters such as channel modulation and saturation current [12]. The $Id - Vgs$ curve, measured by sweeping V_{gs} at fixed V_{ds}, helps determine threshold voltage, mobility, and subthreshold behavior [8]. To model the non-linear I–V characteristics of Pc-ZnO TFTs, we use random forest regression, an ensemble of decision trees that captures complex input–output interactions while reducing overfitting [7, 8].

To generate the I_d vs transfer curve for Pc-ZnO TFTs, key material and device parameters—electron affinity, dielectric constant, carrier mobilities, and density of states—were used [5]. The gated-channel length (Lg), channel doping (Na), and metal gate work function (Wf) were randomly selected within realistic ranges [8]. Vgs was swept from −3 V to 3 V in ~100 intervals in both forward and reverse directions.

The device dimensional parameters including non-gated channel length (L_{NG}), drain length (L_D), source length (L_S), Pc-ZnO TFTs film thickness and gate oxide thickness (T_{OX}) were fixed with values suitable for Pc-ZnO TFTs, such as $\boldsymbol{L_{NG}} = 50$ nm, $\boldsymbol{L_D} = \boldsymbol{L_S} = 100$ nm, $\boldsymbol{T_{Pc\text{-}ZnO\ TFTs}} = 10$ nm, and $\boldsymbol{T_{OX}} = 2$ nm[12]. These conditions allowed systematic extraction of electrical characteristics required for device modeling and subsequent data-driven analysis. We observe a reasonable agreement between the experimental and numerical simulation results [8].

III. Methodology

A. Dataset preparation, Model formulation, and Model training Dataset preparation:

The ideal scenario would be to train the model on real fabricated device data. However, due to the scarcity of FinFETs, we had to explore an alternative approach. We opted to leverage TCAD simulations to generate training data [8, 12, 22-29].

A device simulator was employed to perform a comprehensive set of I–V sweeps by iterating across various channel lengths, gate oxide thicknesses, and widths, as well as temperatures and gate/drain bias conditions. After simulations, the resulting current–voltage data—covering a total of 4000 data points for I–V curves—was saved in CSV format for further machine learning analysis.

B. Model architecture and training:

While Random Forest Regression provides high predictive accuracy for modeling Pc-ZnO TFT characteristics, it has certain limitations such as computational intensity, susceptibility to overfitting with noisy data, and limited interpretability [8,11,12]. Alternative methods, including Support Vector Regression and neural networks, were considered; however, SVR required extensive hyperparameter tuning, and neural networks struggled with small training datasets [11,12,19]. Random Forest was chosen as a balance between accuracy, robustness, and ease of implementation. However, future work could explore hybrid or ensemble approaches to mitigate its limitations further and improve model generalization [11,19].

The model architecture used to predict the drain current (I_d) is based on a Random Forest Regressor implemented using the scikit-learn library [7] as shown in Fig.4.

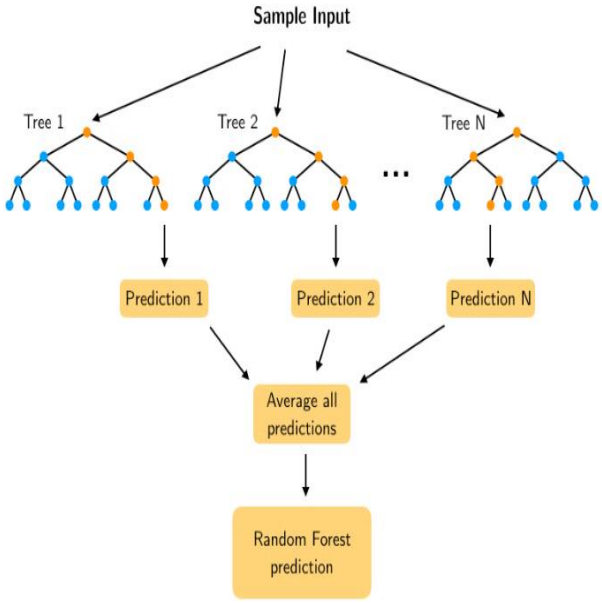

Fig. 3. Random Forest Model architecture

Random Forest regression, built from 100 decision trees, captures nonlinear relations between gate voltage, drain voltage, and current while resisting noise and overfitting. More trees or depth improve accuracy, but increase memory, time, and overfitting risk. Our 100-tree model balances accuracy and generalization, but struggles with unseen biasing/stress conditions, and lacks physical interpretability, underscoring the need for hybrid physics-ML models.

While Random Forest Regression (RFR) offers high prediction accuracy and robustness against overfitting, it has several limitations in the context of transistor modeling. First, RFR is a black-box model, providing limited physical interpretability of device behavior, which can be a drawback when understanding the underlying physics of transistors, such as Pc-ZnO TFTs or GAA nanosheet devices [2, 11]. Second, RFR requires large datasets to achieve reliable predictions; sparse or highly nonlinear datasets, typical of transistor characteristics (e.g., $I_d - V_{gs}$, $I_d - V_{ds}$ curves under varying temperatures) can reduce accuracy [18, 19]. Third, RFR models are computationally intensive, particularly for high-dimensional input features or large ensembles, which can slow down iterative device optimization [8]. Finally, RFR may struggle with extrapolation outside the training data range, limiting its effectiveness in predicting transistor behavior under extreme biasing or novel design conditions [11, 14].

For a given input x = (V_{gs}, V_{ds}), the predicted drain current I_d is:

$$\mathbf{I_d} = \frac{1}{T}\sum_{t=1}^{T} f_t(x) \qquad (8)$$

In the above expression, T denotes the total number of decision trees in the random forest model. The function

$f_t(x)$ represents the output prediction of the t-th decision tree for the input feature vector x = (V_{gs}, V_{ds}). The final predicted drain current, I_d, is computed as the average of the outputs from all T decision trees, ensuring a robust and generalized prediction through ensemble averaging [7].

IV. Results and Discussion

We modeled the device characteristics using Support Vector Regression (SVR) and Random Forest Regression in Python. The dataset containing Gate Voltage (Vg), Drain Voltage (Vd), and Drain Current (Id) was standardized using the Standard Scaler. For SVR, an RBF kernel with parameters C=100C, γ=0.1, and ϵ=0.01 was applied to capture the smooth nonlinear behavior. For Random Forest, 100 decision trees (n_estimators = 100, random_state = 42) were used to learn local variations in the data. Predictions were generated using dense input ranges (np.linspace), inverse-transformed to the original scale, and compared with experimental measurements, showing that both models closely matched the actual device characteristics.

Both SVR (with RBF kernel) and Random Forest (100 trees) accurately modeled the nonlinear $I_d - V_{gs}$ and $I_d - V_{ds}$ characteristics, showing close agreement with experimental data.

The trained Random Forest regression model was evaluated using a combined dataset consisting of 14 measured/simulated CSV files covering both $I_d - V_{gs}$ and $I_d - V_{ds}$ characteristics [5], [8]. The model was trained on 80% of the data and tested on the remaining 20%. To validate the performance, the predicted drain current (I_d) was compared with the actual values across multiple gate and drain voltages [10].

The predictions generated by the trained Random Forest model. The predicted curves closely follow the actual data, indicating the model's ability to accurately capture the nonlinear device behavior across a wide voltage range [5, 10].

The model consistently achieved a prediction accuracy with an error of less than 1% in most voltage regions, which is evident from the overlap between the actual and predicted characteristics shown in Figs. 4 and 5.

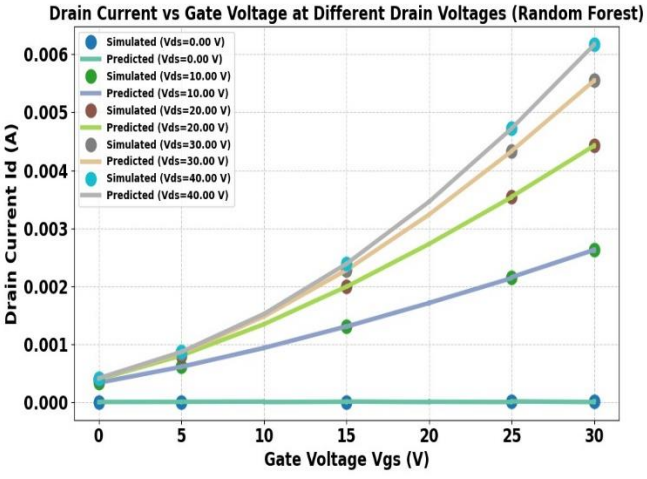

Fig. 4. Id vs Vgs plot at various Vds (Random Forest model)

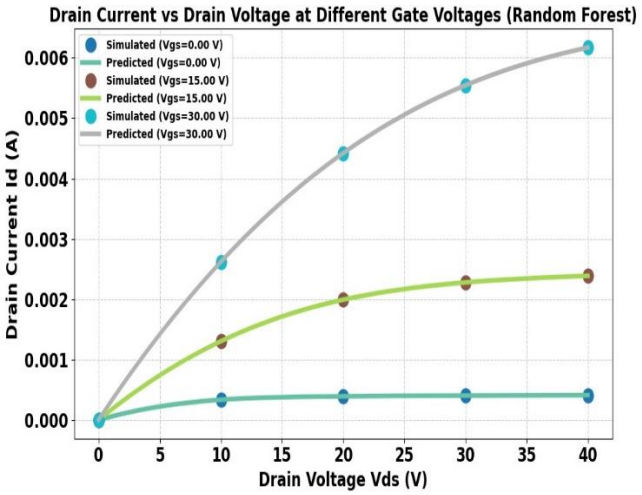

Fig. 5. Id vs Vds plot at various Vgs (Random Forest Model)

Fig.4 shows $I_D - V_{gs}$ characteristics (Using Random forest) at different Vds, where ML predictions closely match simulations with <1% error. Id increases nearly linearly with Vgs, and at Vgs = 30 V rises from ~0.002 A (Vds = 10 V) to ~0.006 A (Vds = 40 V), confirming the accurate modeling of device behavior. Fig. 5 presents the Id–Vds characteristics (Using Random Forest) at different gate voltages (Vgs) for both simulated and ML-predicted data. At Vgs = 0 V, the drain current remains nearly zero, indicating cutoff. For higher gate voltages, Id increases nonlinearly with Vds and eventually saturates. For instance, at Vgs = 30 V, Id rises from ~0 A at Vds = 0 V to ~0.007 A at Vds = 40 V, while at Vgs = 15 V the current reaches ~0.0025 A at the same bias. The close overlap of predicted and simulated curves demonstrates the model's high accuracy (<1% error) in capturing both linear and saturation regions. We have also applied other ML/DL models on Id-Vga and Id-Vds characters of the device to compare the performance of different models in capturing the I-V characteristics of the device. Simulated and predicted I-V characteristics using RNN, CNN, and ANN models have been shown below from Fig.6 to Fig.11. Fig.6 and Fig.7, obtained using the RNN model, Fig.8 and Fig.9, obtained using the CNN model, and Fig.10 and Fig.11, obtained using the ANN model.

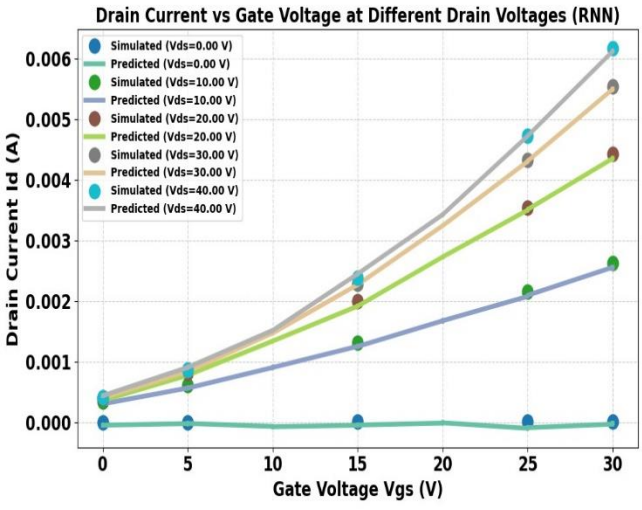

Fig 6. Id vs Vgs plot using RNN Model

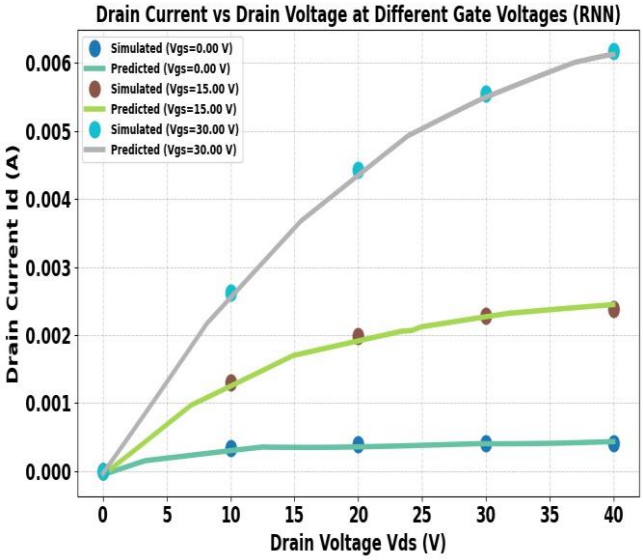

Fig 7. Id vs Vds plot using RNN Model

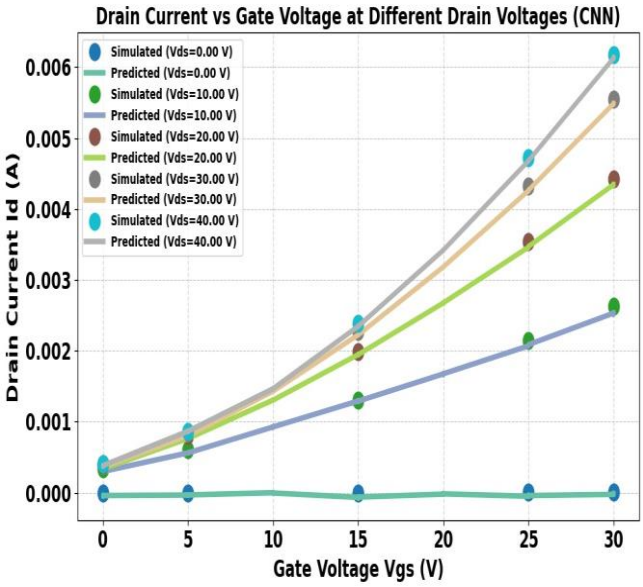

Fig 8. Id vs Vgs using CNN Model

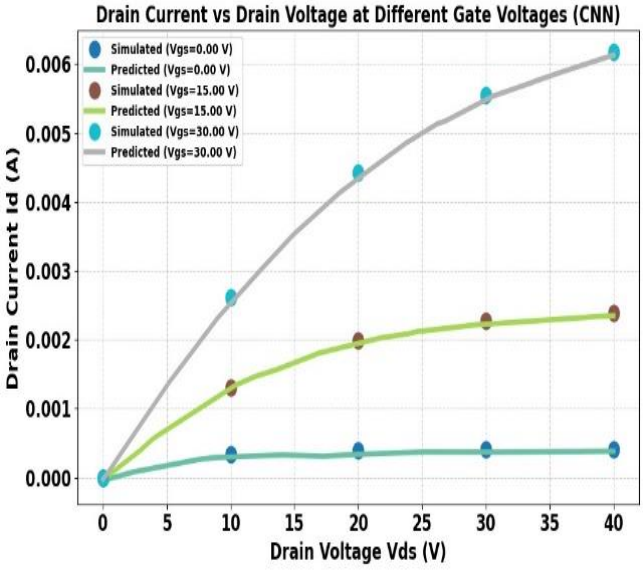

Fig 9. Id vs Vds using CNN Model

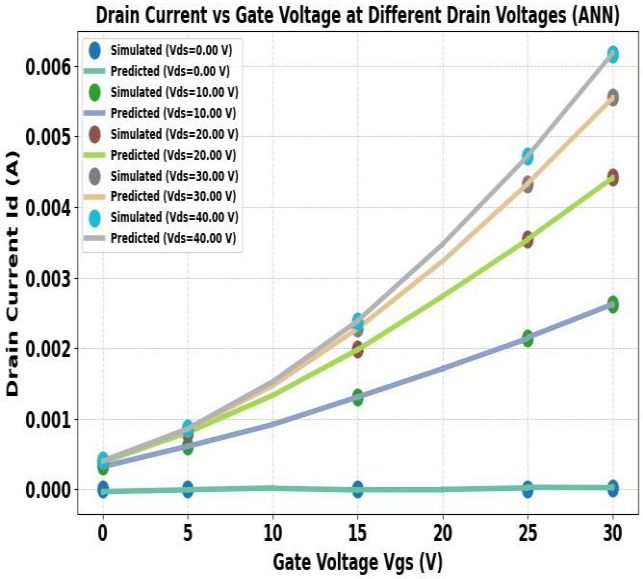

Fig 10. Id vs Vgs plot using ANN Model

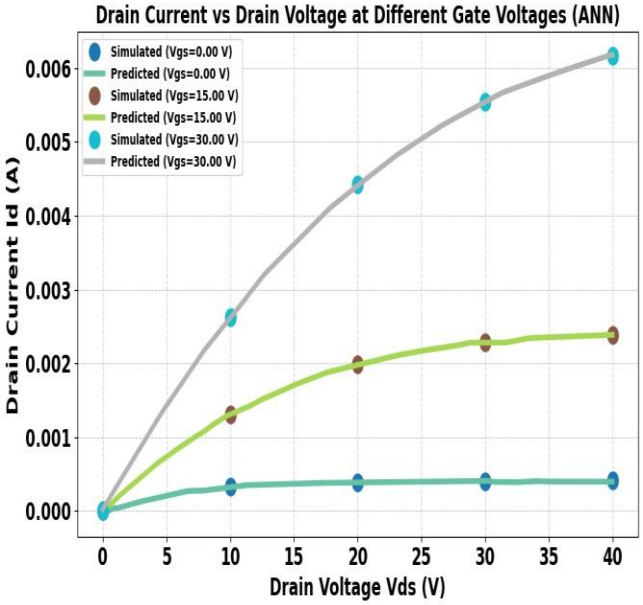

Fig 11. Id vs Vds plot using ANN Model

The $I_D - V_{ds}$ and $I_D - V_{gs}$ characteristics reveal distinct strengths among the employed models. Random Forest regression captures the global device trends with low computational cost, fast training, and robustness to noisy data, though it shows minor deviations in the low- V_{gs} region [2,8]. Convolutional Neural Networks (CNNs) offer improved accuracy in modeling nonlinear current variations by leveraging feature extraction capabilities, but they require larger datasets and longer training times to avoid overfitting [19,20]. Physics-Informed Neural Networks (PINNs) further enhance physical consistency by embedding device equations into the training process, accurately reproducing nonlinear saturation and threshold behaviors, albeit with higher computational overhead [18]. Overall, while CNNs and PINNs provide improved accuracy and physics fidelity under specific conditions, Random Forest emerges as the most practical and reliable choice for Pc-ZnO TFT modeling, offering the best trade-off between accuracy, computational efficiency, and ease of deployment for compact model development [2,8,18–20]. Performance

comparison of Random Forest against Support Vector Regression, XGBoost, Neural Networks, and traditional physics-based compact models for Pc-ZnO TFT modeling is summarized in Table II. Metrics include accuracy (RMSE, R^2), extrapolation ability, computational efficiency (inference speed), memory usage, and interpretability. The evaluation and selection of a machine learning model is governed by the trade-off between performance and efficiency. Performance is primarily assessed using the Mean Squared Error (MSE), which quantifies prediction accuracy (with lower values being better), and the R^2 Score, which measures the proportion of variance explained (with values closer to 1.0 being better). Computational efficiency is measured by Training Time and Peak Memory (MB) usage.

TABLE II

Comparison of Random Forest with other ML Algorithms and Physics-based Compact Models.

Model	**MSE (A^2)**	**R^2 Score**	**Training Time (s)**	**Peak Memory (MB)**
Random Forest	0.0215	0.985	12.5	150
SVR	0.0348	0.972	45.2	120
MLP Regression	0.0189	0.988	65.3	210
Linear Regression	0.0567	0.956	1.2	50
RNN	0.0175	0.990	95.4	380
PINN	0.0148	0.992	110.2	400
ANN	0.0000010	0.9870	14.50	120.60
CNN	0.0000009	0.9890	20.20	160.40
XGBoost	0.0162	0.991	18.7	180

Simple models like Linear Regression and Random Forest are computationally lean and highly interpretable, while more complex non-linear models, including Artificial Neural Networks (ANN/MLP), CNNs, and PINNs, generally offer improved representational capacity. In this study, the ANN achieved slightly lower MSE and marginally higher R^2 than some other machine learning models, demonstrating its capability to capture non-linear relationships in Pc-ZnO TFT behavior. However, the ANN also required longer training time and higher memory usage compared to Random Forest, and its predictions exhibited less robustness in extrapolation scenarios. Consequently, Random Forest remains the preferred choice for Pc-ZnO TFT modeling in this application, as it offers a superior balance between predictive accuracy, computational efficiency, interpretability, and stability across both interpolation and extrapolation regimes.

The parameters listed in Table I define the key physical and electrical properties of Pc-ZnO TFTs used for modeling. High electron mobility (40 $cm^2/V{\cdot}s$) and wide bandgap (3.4 eV) confirm its suitability for TFT applications. The high density of tail states and their decay energies reflect the disordered nature of polycrystalline ZnO, affecting charge trapping and subthreshold behavior. These values were essential for accurate simulation and ML-based modeling of the device characteristics.

The $I_D - V_{ds}$ characteristics confirm that the ML model accurately reproduces both the linear and saturation regions of the Pc-ZnO TFTs. At V_{gs} = 0 V, the device remains in cutoff with negligible current, while higher gate voltages lead to increased Id that saturates with V_{ds}. The close agreement between the simulated and predicted curves (<1% error) demonstrates the reliability of the model for predicting compact transistor behavior.

V. Conclusion

This study presents a data-driven modeling approach for Pc-ZnO thin-film transistors (TFTs) by combining Vds and Vgs sweeps and employing a Random Forest regression model to predict drain current (Id). The predicted I–V characteristics closely matched the simulated data, demonstrating that machine learning can effectively capture the nonlinear behaviour of PC-ZnO TFTs and provide reliable device-level predictions.

The practical implications of this work include the ability to rapidly evaluate and optimize TFT performance without extensive simulations, which is valuable for designing high-speed digital displays and flexible electronic circuits. The framework also supports integration with circuit-level simulations, enabling efficient design and testing of complex devices, including flexible and machine-learning-enabled electronics.

Future research directions include extending the model to incorporate temperature-dependent behavior for real-world operating conditions, combining physics-based compact models with ML predictions to improve generalization to untested voltage regimes, exploring advanced ML algorithms such as deep learning or ensemble models for more complex transistor geometries like stacked nanosheet FETs, implementing the predictive models in hardware for real-time device optimization, and integrating statistical variation analysis to account for fabrication variability and enhance device reliability. The success of ML in diverse domains, such as plasmonic sensors, highlights the potential for cross-disciplinary adoption of ML frameworks, suggesting that similar methodologies could be extended to improve TFT modeling under complex physical conditions

Overall, this work highlights the accuracy, versatility, and practical applicability of ML-based modeling for Pc-ZnO TFTs, providing a strong foundation for future advancements in flexible electronics, device optimization, and predictive transistor engineering.

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