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A Highly Efficient Nanoscale Demultiplexer Architecture based on Quantum-Dot Cellular Automata

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***Abstract*-This paper presents the design of a demultiplexer (DMUX) structure using Quantum-dot Cellular Automata (QCA) technology. A demultiplexer is a fundamental circuit that receives information from a single input line and routes it to one of several output lines, with the selected output determined by the control inputs. Widely employed in communication systems, demultiplexers enable the transformation of serial data streams into parallel outputs. In this work, an optimized architecture for a 1:2 QCA demultiplexer is proposed, characterized by simplicity, efficiency, and reliability, with the added capability of implementing a wide range of logical functions. Furthermore, a novel 1:4 QCA demultiplexer is developed based on the proposed structure, eliminating the need for coplanar cells or crossover wires. Simulation results confirm the superior performance of the proposed architectures in terms of reduced cell count, area, and latency. Specifically, the 1:2 design requires only 17 QCA cells, occupies 0.01 µm², and exhibits a delay of 0.25 clock cycles, while the 1:4 demultiplexer requires 74 QCA cells, occupies 0.07 µm², and achieves a delay of 3 clock cycles.**

***Index Terms*- Demultiplexer, Majority voter, Quantum-dot Cellular Automata, Crossover, Coplanar.**

I. INTRODUCTION

Quantum-dot cellular automata (QCA) is an emerging nanotechnology that offers a promising alternative to conventional CMOS technology for implementing digital circuits at the nanoscale. First introduced in the early 1990s, QCA exploits the position of electrons within quantum-dot cells to represent binary information, thereby eliminating the need for current flow as in traditional transistor-based logic. Instead of relying on transistors, QCA uses the Coulombic interactions between neighboring cells to perform computation and signal transmission, enabling ultra-low power consumption and extremely high device density. With feature sizes potentially scaling down to a few nanometers, QCA has gained significant attention in recent decades as one of the most viable post-CMOS computing paradigms.

Due to its inherent advantages, QCA has been extensively explored for a wide range of applications, including logic gates, arithmetic circuits, memory elements, and complex architectures such as multiplexers, demultiplexers, and processors. Its potential for ultra-fast switching, reduced interconnect delay, and energy-efficient operation makes it highly relevant for the design of nanoscale computing systems where conventional CMOS faces scaling and power dissipation challenges. Moreover, the ability of QCA to implement highly compact, regular, and fault-tolerant architectures positions it as a key enabler for next-generation nano-electronic systems. In this context, designing efficient QCA-based demultiplexers is particularly important, as they are essential building blocks for signal routing, data distribution, and communication in nanoscale circuits.

Due to its advantages, such as rapid speed, small size, and low energy consumption, QCA technology stands out as one of the selected methods for addressing the challenges faced by nanometer-scale CMOS devices. Some of these obstacles encompass high power density levels, elevated leakage currents, and substantial lithography costs. In QCA circuits, which are being explored as potential substitutes for CMOS technology, information processing revolves around cell polarization, which is subsequently communicated to neighboring cells through Coulomb contact. The high device density [1], ultra-low power efficiency [2], and rapid computing performance [3-6] exhibited by these nanostructures have been extensively demonstrated.

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Consequently, QCA-based logic circuits have garnered significant attention in recent years.

Numerous endeavors have been undertaken to utilize these nanostructures for implementing crucial components of Combinational Circuits, including XOR, X-NOR gates [7–11], multiplexers, demultiplexers [12–18], Adders, Subtractors, RAM cells, and ALU units.

Among the various circuit architectures explored using QCA, demultiplexers play a crucial role as fundamental data-routing elements in communication and computing systems. They are widely used in memory addressing, signal distribution, and interconnection networks, where efficient and reliable data transfer is essential. As the demand for nanoscale integration grows, QCA-based demultiplexers have been the subject of extensive research aimed at reducing circuit area, minimizing latency, and improving overall stability. Several designs have been proposed in the literature with varying trade-offs between complexity, performance, and robustness. Demultiplexer is one of the important parts of the nano-router building blocks and to imitate the calculator circuit, a demultiplexer combines adder, subtractor, multiplexer, and divider circuits into a single circuit. The data is taken via input lines, and sent to the 2N output at a time, based on N selector signals. Output equation of 1:2 demultiplexer is Out0 = $S\bar{}$.IN, Out1 = S.IN, where S = 0 means the input data transferred to output 0 and if S = 1 means the input data is sent to the output 1. In QCA technology, several designs and architectures for demultiplexers have been published.

A systematic review of the existing demultiplexer architectures is necessary to highlight their strengths and limitations, and to position the proposed nanoscale demultiplexer within the context of ongoing advancements in QCA-based circuit design. In [19], the authors propose a fault-tolerant 1:2 QCA demultiplexer using an inverter and a two-input AND gate. The design leverages cell redundancy to enhance robustness against common defects such as missing, dislocated, extra, and misaligned cells. However, the approach remains limited in scalability, as it only addresses a basic 1:2 demultiplexer structure rather than larger and more complex architectures. The demultiplexing method presented in [20] focuess on energy dissipation and cost metrics, using QDE and QCAPro simulation tools. Results show that the proposed designs achieve very low energy dissipation and favorable cost functions, highlighting their efficiency for nanoscale systems. However, the work is limited to small-scale blocks and relies on simulations at low operating temperatures (2 K), which may restrict practical applicability.

Khan an Arya have proposed QCA layouts for a 1:2 multiplexer and 1:2 demultiplexer, showing low energy dissipation and evaluated through both QDE and QCAPro with multiple cost functions [21, 22]. Meanwhile, Sharma and Kaushil have proposed a novel area-efficient 1:2 QCA demultiplexer using only 11 cells, achieving significant reductions in layout area, cost, and power dissipation compared to prior designs [23]. While their results demonstrate strong efficiency and energy savings, the study is limited to a basic 1:2 architecture, leaving scalability to larger demultiplexers unexplored. Similar structures have been proposed in [24-30].

This study provides a 1:2 demultiplexer with an optimum structure and suggested architecture is used to implement the 1:4 demultiplexer. Concerning size, speed, and intricacy, the suggested architecture provides several advantages over the topologies reported in the literature. The novelty of this work lies in proposing an optimum QCA-based demultiplexer architecture that is both simple and highly efficient, requiring fewer cells, smaller area, and lower latency than existing designs. Unlike many prior approaches, the 1:4 demultiplexer is implemented without coplanar cells or crossover wires, significantly improving reliability and scalability. Additionally, the architecture is versatile, as it can be extended to generate a range of logical functions, making it a flexible building block for nanoscale communication systems.

II. QCA Basic Elements

The basic structure of a QCA cell is illustrated in Fig. 1 [31, 32]. Each cell consists of four quantum dots arranged in a square configuration and two mobile electrons, which can tunnel between the quantum dots. Due to electrostatic repulsion, the electrons occupy antipodal sites within the cell. Unlike conventional electronics, where current flow represents information transfer, QCA operates through Coulombic interactions, whereby the state of one cell influences its neighboring cells, enabling data propagation. The system has two energetically stable configurations, as shown in Fig. 1, corresponding to distinct electron arrangements. The polarization of a QCA cell, defined by Equation (1), determines whether the cell represents a binary "0" (−1 polarization) or binary "1" (+1 polarization) based on the positions of the electron pair [33, 34].

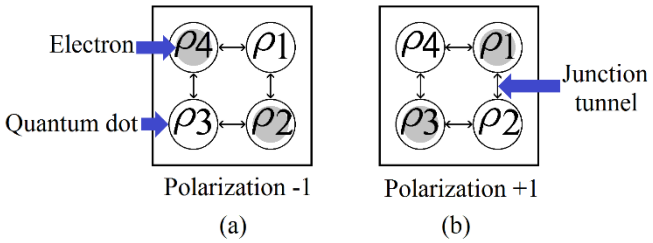

Fig. 1. Structure of a basic QCA cell and cells polarization in QCA technology (a) Polarization -1 refers to 0 (b) Polarization +1 refers to 1.

TABLE I
Three-input Majority Voter Truth Table

IN			OUT
Z	Y	X	O
0	0	0	**0**
0	0	1	**0**
0	1	0	**0**
0	1	1	**1**
1	0	0	**0**
1	0	1	**1**
1	1	0	**1**
1	1	1	**1**

The fundamental building blocks of QCA technology are the majority voter (MV) gate, the inverter gate, and the binary wire. The MV is a three-input device realized with a five-cell configuration, as illustrated in Fig. 2(a). Inputs are applied through cells A, B, and C, while the central cell acts as the device cell, adopting the polarization of the majority of the inputs. The output cell (O), positioned on the right, replicates

the polarization of the device cell. The complete truth table of the MV gate is presented in Table I, while Fig.s 2(b) and 2(c) demonstrate how the MV can be configured to implement 2-input AND and OR logic functions, thereby covering all possible input–output combinations of the majority voter.

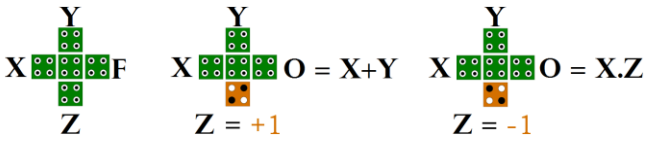

Fig. 2. Structure of (a) Majority voter (b) Majority voter as an AND logic gate (c) Majority voter as an OR logic gate.

The QCA wire is shown in two different configurations in Fig. 3. Although in QCA technology wires contribute to information transfer from one part of the circuit to another, they can conduct certain computations on the data to be sent. The other basic logic gate in QCA is the inverter gate. It takes the logic from the input and creates the logic's complement on the output. The output equation of the inverter gate is $A = \bar{A}.Clk$. Inverter gates can be layout in a variety of methods, but the structures depicted in Fig. 4 are regarded to be as reliable as inverter gates.

Fig. 3. Schematic of a) Normal wire built with normal cells, (b) Rotated wire built of rotate cells.

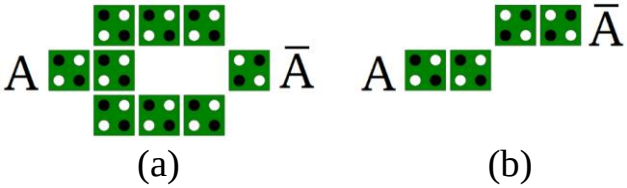

Fig. 4. Structure of a (a) QCA inverter gate with two paths, (b) QCA operational inverter gate.

III. Clocking in QCA

In conventional CMOS technology, the clock is employed to control the timing of sequential circuits. In QCA, however, the clock not only governs switching but also provides the necessary output gain [35, 36]. Clock signals regulate electron tunneling by modulating the potential barriers between quantum dots, and they are generated using electric fields supplied through CMOS or carbon nanotube (CNT) wires embedded beneath the QCA surface [37]. The maximum number of cells that can be assigned to a single clocking zone is determined by Eq. (1), where E_k denotes the kink energy, k_B is the Boltzmann constant, and TTT is the operating temperature in Kelvin. [34].

$$Number\ of\ Cells \leq e^{(Ek/KB.T)} \quad (1)$$

As indicated in Fig. 5, the clocking technique is made up of four clock pulses with the same frequency that one clock signal is regarded as the reference (clock = 0), while the others are delayed one-quarter of the period. Each clock pulse has four phases: switch, hold, release, and relax. With a phase shift of 90 degrees. Clocking is accomplished by electrostatically switching the cell from its null state, in which it contains no binary data. The condition of a cell is dictated by its surroundings. The whole QCA circuit is separated into clock zones, with each clock signal assigned to its zone. The cells of each clock zone transit through all four phases of that clock zone during the communication process. After these four processes, the information is sent.

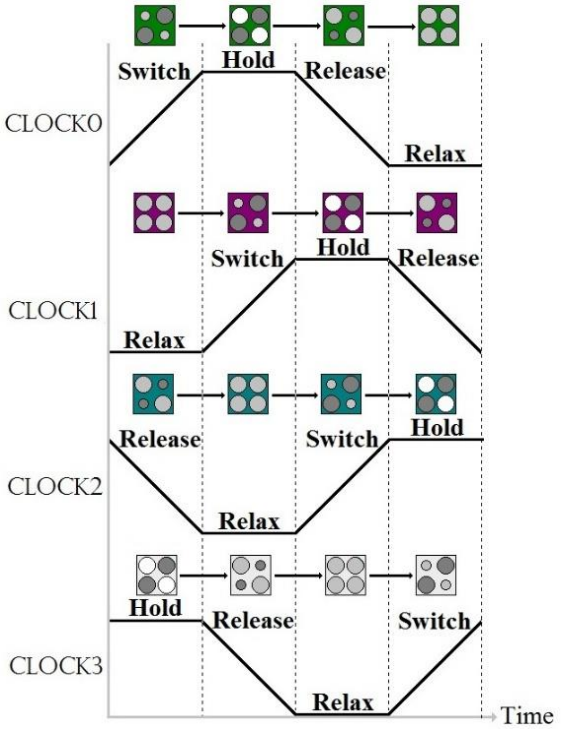

Fig. 5. Clocking schemes and a variety type of cells in QCA technology that use for information transfer.

IV. Previous Works

Different architectures and implementations for QCA-dependent demultiplexers have been discussed in this section. Demultiplexer circuit takes information from its input and sends them to the output lines, where at each time one of the 2N outputs depending on N selector signals receives input data. In [35] proposed a new modular approach for designing a 1:2N demultiplexer. This method simplifies the process of designing high-order demultiplexers. As a building block, 1:2 QCA demultiplexer architectures are supplied, followed by 1:4 and 1:8 demultiplexers. Any 1:2N demultiplexer that has been schematized using the recommended approach may easily be upgraded to a bigger 1:2N demultiplexer. A lesser cell count and a smaller area are used in this suggested technique.

A QCA 1:4 demultiplexer is a necessary component of a QCA nano-router device suggested in [32]. A large number of gates are used in the implementation of this circuit. To deal with the problem of line crossing, a design with several layers was used, with no interference from cells. This design allows the nano-router to communicate at a faster rate. Ahmad [37] has presented a unique notion of a 1:2n demultiplexer based on QCA technology. The present execution is primarily focused on improving efficiency and reducing circuit complexity. Two inverters and four three-input AND gates were required to create an optimum 1:4 demultiplexer using

this layout. The suggested designs have evolved in terms of space utilization and complexity.

Many other topologies have been presented in the literature [38-44]. For instance, to make a QCA-based Nano-calculator, Chakrabarty et al. built a 1:4 demultiplexer [41]. To imitate the calculator circuit, this demultiplexer combines adder, subtractor, multiplexer, and divider circuits into a single circuit. Three clock zones are employed to complete a full cycle in the described demultiplexer, which is dependent on a multilayer crossover method. The suggested configuration has a larger overall area and a greater QCA cell number. 1:2 demultiplexers have two majority voters, and one to four demultiplexers have eight majority voters in this configuration. The multilayer crossover was avoided in the suggested designs.

V. The Proposed Topologies

Table II and Fig. 6 show the truth table and configuration of the recommended one-to-two demultiplexer respectively. The suggested structure utilizes two majority gates with AND logic implementations to optimize device density, layout area, number of QCA cells, and computation velocity in a single layer. There is no need to rotate or crossover cells and the suggested arrangement is single-layer and consists of 17 QCA cells, with a total size of 0.01 µm2. Furthermore, it utilizes one phase of the clock for producing valid output. The layout of the proposed structure demonstrates in Fig. 7.

TABLE II
Truth Table for QCA-DMUX of 1:2.

S	IN	Out1	Out0
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	0

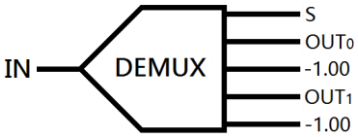

Fig. 6. Schematic circuit of the proposed 1:2 QCA-DMUX.

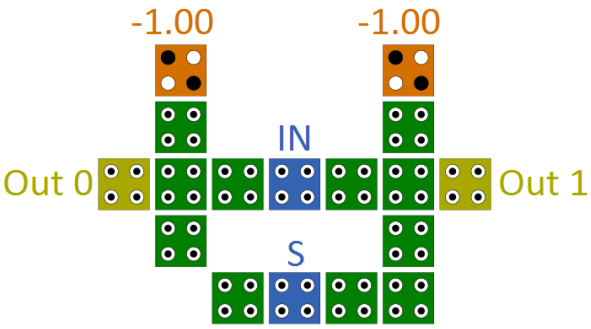

Fig. 7. The layout circuit of the proposed 1:2 QCA-DMUX.

Four outputs (Out0, Out1, Out2, and Out3), 1 input (IN), and 2 selector lines (S0S1) make up the 1:4 DEMUX. The suggested structure employs three 1:2 demultiplexer blocks, as shown above. Table III shows the truth table of a 1:4 demultiplexer, when S0S1=00, 01, 10, and 11, the Out0, Out1, Out2, and Out3 get the input data respectively. The 1:4 demultiplexer architecture is implemented in a single layer without the application of crossover or rotate cells, and the suggested structure has 74 QCA cells and takes up 0.07 µm2 of space. Furthermore, it makes utilization of three phases of the clock to provide legitimate output. Fig. 8 and Fig. 9 shows the schematic and the configuration of the suggested demultiplexer architecture respectively.

TABLE III
Truth Table for QCA-DMUX of 1:4.

S0	S1	IN	Out3	Out2	Out1	Out0
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	0	0
0	1	1	0	0	1	0
1	0	0	0	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

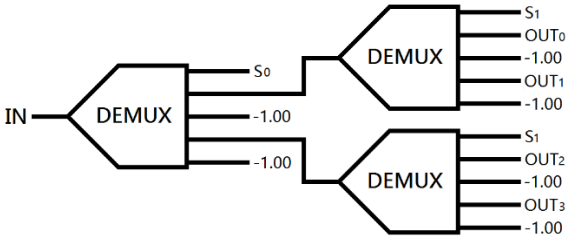

Fig. 8. Schematic circuit of proposed 1:4 QCA-DMUX.

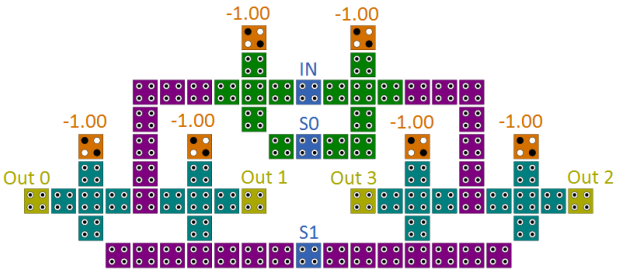

Fig. 9. Layout structure of proposed 1:4 QCA-DMUX.

VI. Results and Comparisons

The input and output waveform simulations of the proposed 1:2 and 1:4 demultiplexers illustrate in Fig. 10 and Fig. 11 respectively. Table IV and Table V provide a comparison of performance between the proposed design and earlier designs. QCA Designer tool and Bistable Approximation engine by the default settings were used to create all of the proposed circuits and results. In QCA circuits, information propagates as the polarization of one cell influences its neighboring cells. At certain points, wire crossings are required to facilitate signal routing. The primary crossover techniques in QCA include planar, multi-layer, and logical crossovers. Planar crossovers typically employ a combination of regular and rotated cells, multi-layer

crossovers rely on multiple physical layers, and logical crossovers achieve wire intersection by utilizing non-consecutive clock phases. To evaluate the designing efficiency, the cost function known as the generalized cost function for semiconductor QCA is used, where the number of majority gates (M), inverter gates (I), latency (T), and the number of wire crossing (C) coplanar crossing Ccp or multilayer crossing Cml are considered as an evaluation parameter. The generalized QCA evaluation cost function is determined using Eq. (3). The weight metrics for majority gate, wire crossing, and delay, respectively, are the exponential values α, β, and δ Which are considered 2. The cost of multilayer crossing Cml is three times higher than the cost of coplanar crossing Ccp when the manufacturing complexity is taken into account. Table IV displays the results of comparing the proposed 1:1 demultiplexer to its existing counterparts, while Table V shows the results of comparing the proposed 1:4 demultiplexer to its current equivalents [34].

$$Cost_{QCA} = (M^{\alpha} + I + C^{\beta}) \times T^{\sigma},\ \alpha, \beta, \sigma \geq 1 \quad (2)$$

Based on the comparison given, the offered designs achieve superior results in terms of the number of cells and betterment in the occupied area. Additionally, as compared to its competitors, the provided one to four demultiplexers has a lower QCA cost. Using the same approach, proposed optimum architectures may be utilized to construct higher-order demultiplexers to tackle the problem of latency.

TABLE IV
Performance comparison of the proposed 1:2 Demultiplexer with related works.

1:2 DMUX	Number of cells	Area (μm²)	Crossover type	Clock zone	Cost	Delay
[39]	56	0.08	Coplanar	4	144	1
[31]	27	0.04	Coplanar	2	24	0.5
[35]	23	0.03	Without	2	20	0.5
[27]	21	0.03	Without	2	20	0.5
[33]	21	0.03	Without	2	20	0.5
[26]	21	0.02	Without	2	20	0.5
Proposed	17	0.01	Without	1	5	0.25

TABLE V
Comparison of the proposed 1:4 Demultiplexer in terms of performance with the previous works.

1:4 DMUX	Number of cells	Area (μm²)	Crossover type	Clock zone	Cost	Dela y
[43]	404	0.60	Coplanar	9	1053	2.25
[44]	212	0.31	Coplanar	8	1056	2
[40]	188	0.22	Coplanar	4	2096	1
[38]	149	0.19	Multilayer	8	3520	2
[41]	110	0.14	Multilayer	3	900	0.75
[42]	125	0.15	Without	6	___	1. 5
[37]	187	0.18	Coplanar	7	1421	1.75
[36]	92	0.12	Coplanar	4	656	1
Proposed	74	0.07	Without	3	351	0.75

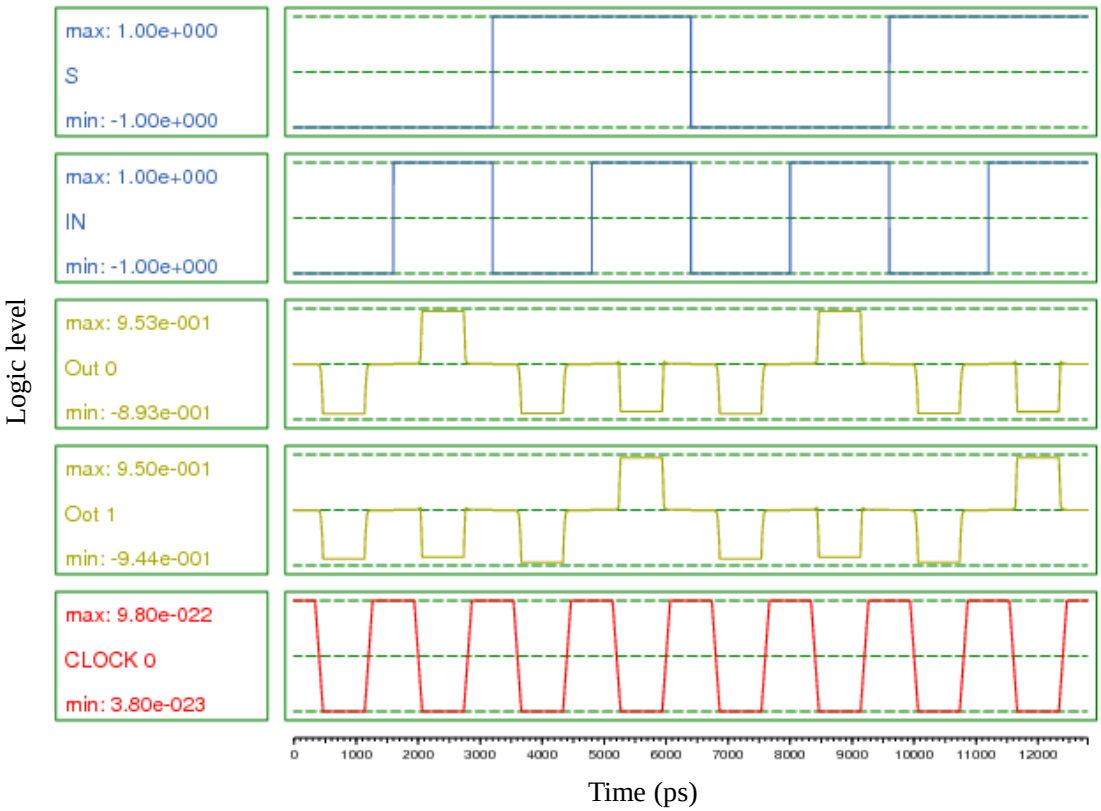

Fig. 10. The proposed 1:2 QCA-DMUX simulation result.

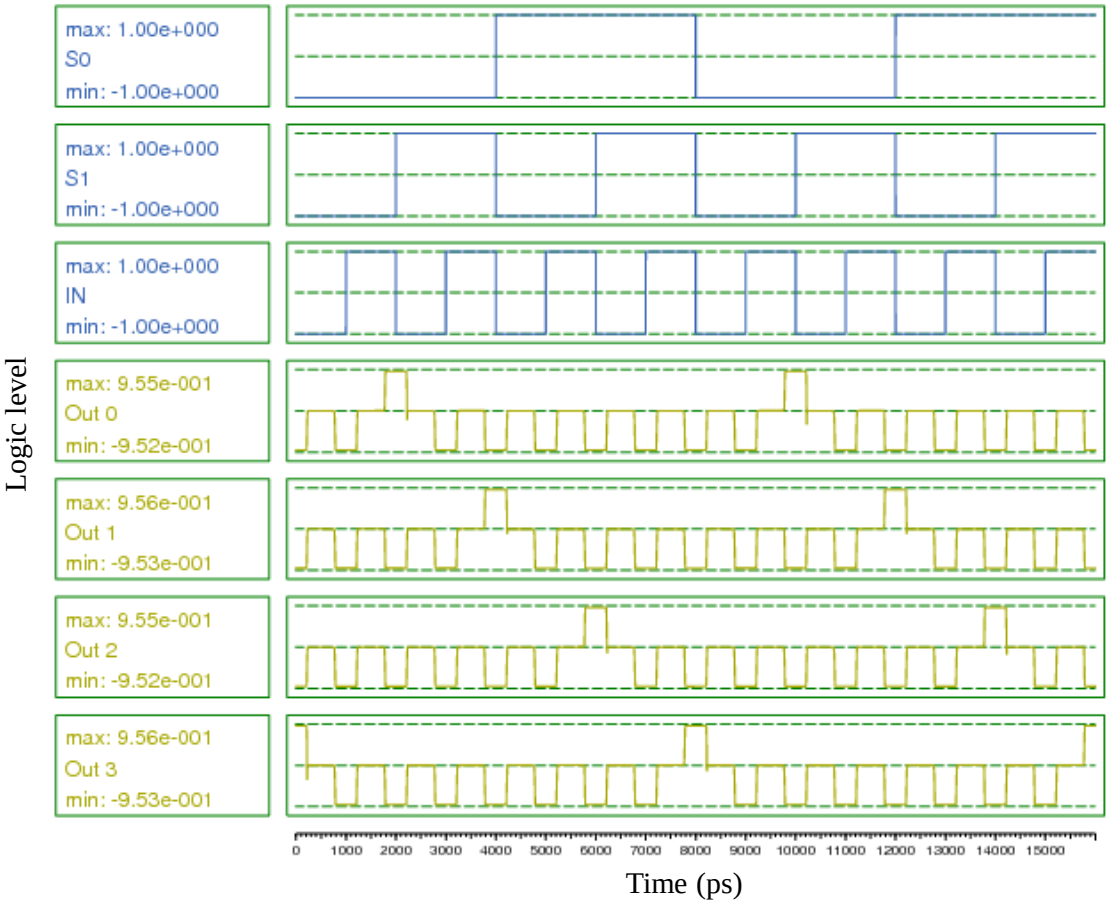

Fig. 11. The proposed 1:4 QCA-DMUX simulation result.

VII. CONCLUSION

This research presented an optimized design for a 1:2 QCA demultiplexer, which serves as the foundation for constructing a novel 1:4 demultiplexer architecture using the Bistable Approximation engine. The proposed circuits were modeled and validated with the QCADesigner tool. A key advantage of both designs is their ability to achieve correct functionality without the need for crossover wires, coplanar arrangements, or rotated cells, thereby enhancing reliability and simplicity. Compared to existing demultiplexer implementations, the proposed architectures are more cost-effective and less complex, while simulation results confirm significant improvements in terms of cell count, latency reduction, and elimination of wire crossings.

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