Semnan University

Journal of Modeling & Simulation in Electrical & Electronics Engineering (MSEEE)

Journal homepage: **https://mseee.semnan.ac.ir/**

ISSN: 2821-0786

Asymmetric Voltage Multiplied Non-Isolated Bidirectional DC-DC Converter with Soft-Switching and High Gain

Mahdi Madadi [1], Mostafa Jazaeri[2*] and Hamed Molla-Ahmadian[3]

***Abstract*-This paper introduces a novel bidirectional DC-DC converter (BDC) that has a high gain of voltage, soft switching capability, and minimal ripple current on the low-voltage side (LVS). The suggested converter consists of an improved two-phase buck-boost converter, an Asymmetrical Voltage Multiplier cell, and a coupled inductor to provide a high-voltage gain converter. This paper offers a comprehensive theoretical examination of the converter. The converter elements, performance, and switching intervals provide suitable conditions for conducting the switches with zero voltage switching (ZVS) conditions. Due to the implementation of soft switching, the efficiency is increased, and no voltage spikes occur across the switches. The simulation was executed to design a converter and analyze its performance using the PSIM. The suggested converter offers an ultra-high voltage converting gain in both boost and buck operation modes. A laboratory prototype with a power of 300W is implemented to validate the performance of the converter. The presented experimental results outline a low-side voltage of 50V DC and a high-side voltage of 300V DC during the step-up operation.**

***Index Terms*- Asymmetrical Voltage Multiplier, DC-DC Converter, High Gain, Soft Switching, Non-Isolated**.

I. INTRODUCTION

Nowadays, the increasing use of renewable energy in existing power systems has greatly enhanced the importance of power electronics converters. Bidirectional DC choppers are useful in fields like renewable energy technologies, microgrids and electric cars. Many studies have been carried out on different topologies and techniques for using DC choppers as part of energy storage systems. Bidirectional DC choppers obtain significant voltage gain in both buck and boost modes, facilitating effective power conversion and transmission, rendering them appropriate for renewable energy uses. They can convert a low voltage such as 12, 24, or 48V to a high voltage to provide a DC link for an inverter and also convert high voltage to low voltage due to bidirectional capability. As a result, bidirectional converters with high voltage step-down/step-up gain are beneficial for use in renewable energy storage applications to adjust the power and voltage values between the low voltage level and the high voltage connections.[1]–[4]

Generally, bidirectional converters are categorized into two groups: non-isolated and isolated converters. A solution to obtain high voltage gain is to use an isolated transformer. Electrical isolation is one of the most popular methods for providing high voltage conversion by adding a degree of freedom to the converter voltage gain equation. Thus, the desired voltage gain is achieved by selecting the appropriate coil turns ratio. These converters can be utilized for applications that require a wide range of input source variations and load regulation. These converters find use in various applications. However, they frequently encounter practical issues such as high weight, magnetic interference, and the necessity of an active or passive clamp [5]. When the voltages on either side of the dual-active-bridge BDC are not matched, it can lead to problems such as high circulating currents, elevated turn-off power losses, and the loss of soft-switching capability. These challenges, in turn, can result in a significant decrease in conversion efficiency [6]–[8].

A straightforward approach to achieving bidirectional

Received; 2025-09-06 Revised; 2025-09-26 Accepted; 2025-10-14

[1] Faculty of Electrical and Computer Engineering, University of Semnan, Semnan, Iran.
[2] Faculty of Electrical and Computer Engineering, University of Semnan, Semnan, Iran.
[3] Department of Electrical Engineering, Khorasan Institute of Higher Education, Mashhad, Iran.
*Corresponding author: mjazaeri@semnan.ac.ir

Cite this article as:
Madadi, M., Jazaeri, M. & Molla-Ahmadian, H. (2025). Asymmetric Voltage Multiplied Non-Isolated Bidirectional DC-DC Converter with Soft-Switching and High Gain. *Journal of Modeling & Simulation in Electrical & Electronics Engineering (MSEEE)*. Semnan University Press. *6 (1)*, 21-32.
DOI: https://doi.org/10.22075/mseee.2025.38925.1226

power exchange is by using a boost converter, where the diode is replaced with a switch, allowing for bidirectional power flow. However, this approach isn't ideal for high step-down/step-up applications due to several challenges. Firstly, while high switching frequencies can enhance dynamic response and power density while reducing passive element size, they also increase switching losses and worsen diode reverse recovery, leading to lower converter efficiency. Using slow-power-switch diodes as rectifying elements exacerbates the reverse recovery issue and results in high voltage and current stresses in semiconductors. Additionally, high switching frequencies may cause electromagnetic interference, negatively impacting other devices.

Second, most industrial applications require high voltage conversion rates. Low-gain converters, such as conventional buck-boost converters, must operate at duty cycles close to zero/one to achieve high voltage step-down/step-up gains, which increases current stress in switches and diodes and raises conduction losses.

Third, to minimize conduction loss and semiconductor costs, low switch voltage stress is crucial, and the voltage level significantly influences the correct switch selection [9]–[11]. In [12]-[14], several high-gain converters are introduced that employ multilevel converters.

This method provides high gain and decreases the switches' voltage stress however the quantity of switches has increased. This results in increase in the cost and complexity of the control method, complicating the topology and control circuit.

In addition, switched capacitor (SC) circuits are used to increase the voltage rating [15]–[17]. The voltage gain is increased by this method but some converters based on SCs suffer from the high current transient issues. This problem has a negative effect on power density and decreases the efficiency [10], [18].

In [19], the voltage gain is achieved using a converter consisting of two boost converters. To increase the efficiency of traditional buck-boost converters, a circuit composed of a cascaded step-up-step-down converter along with an extra capacitor is suggested [20]. A bidirectional two-phase topology with high voltage gain is presented in [21]. In [22], a DC chopper with bidirectional functionality and soft switching capability is suggested**.** The voltage gain rises but is contingent on the switching frequency**.**

The paired inductors are employed to achieve a notably high step-down gain in [8], [10], [22]–[26]. This method has several benefits. The high step-down of step-up gain can be achieved by using a turn ratio. Furthermore, they can be controlled by conventional PWM control. In [10] high voltage gain is provided by employing a voltage doubler cell connected the buck-boost BDC. The coupled inductor is used to increase voltage gain based on the turn ratio. A high voltage gain BDC with a coupled inductor is proposed in [22], but the voltage gain is limited compared to the others. The bidirectional interleaved buck-boost linked to a dual active half-bridge provides significant voltage gain by utilizing a coupled inductor as shown in [23]**.** In [24], a method of combining voltage amplification modules and coupled inductors is used to achieve a high step-up/down voltage conversion. In [25], a proposal includes a two-phase converter on the low voltage side alongside a parallel high voltage series converter that features coupled inductors to obtain significant voltage amplification. The topology proposed by [26] provides high voltage gain by employing two coupled inductors. In [27], a proposal features a bidirectional design with high gain for a BDC converter, integrating a dual active half-bridge (DAHB) with a high-gain interleaved DC-DC converter through the use of a coupled inductor.

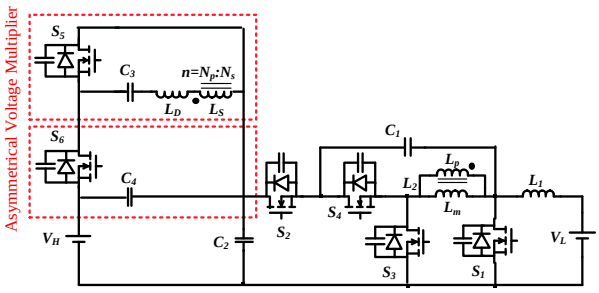


Fig. 1. The schematic of proposed converter.

The design provides multiple important benefits, such as high voltage amplification, two-way power flow, and soft switching to minimize energy losses. Ref. [28] employs two coupled inductors to achieve a high voltage gain. Although this results in a higher voltage gain, it also increases the overall volume of the passive components.

This paper proposes a non-isolated bidirectional DC-DC converter that has soft switching capability for the keys and offers higher voltage gain than competitors by using an asymmetric voltage multiplier cell.

II. Proposed Converter

This converter, obtained from the acknowledged converters in [11] and [24], is illustrated in Fig. 1. The suggested converter enhances the voltage gain in comparison to [11] and [24]. The system includes of a two-phase step-up-step-down converter composed of switches S_1, S_2, S_3 and S_4, capacitors C_1 and C_2 and inductor L_1 at the low-side input. The converter consists of a voltage amplification cell consisting of capacitors C_4 and C_3, switches S_5 and S_6 and an inductor L_D, forming an asymmetric voltage gain converter. Additionally, the coupled inductor, L_2, is characterized by its primary winding, np, a secondary winding, ns and a magnetic inductance, L_m. The leakage inductance of the coupled inductor is combined with an L_D inductance structure.

A. Operating Principle

Switches S_2 and S_4 operate in reverse to switches S_1 and S_3. The duty cycle for switches S_2 and S_4 is identical to the value of D. α is the amount of overlap for S_3 and S_1, which is defined as α=D-0.5. Switches S_6 and S_5 operate in reverse of each other with a duty cycle of 0.5. Dφ represents the phase difference between switches S_5 and S_1, While the S_1 gate pulse has a phase difference of π with the S_2 gate pulse (along with S_3 and S_4). This converter functions across twelve intervals during one switching period. The various states during a switching period for Dφ >α are detailed below.

For easier analysis of the steady state of the proposed converter, the following assumptions are made:

- The ripple current of inductor L_1 is ignored because it is sufficiently large

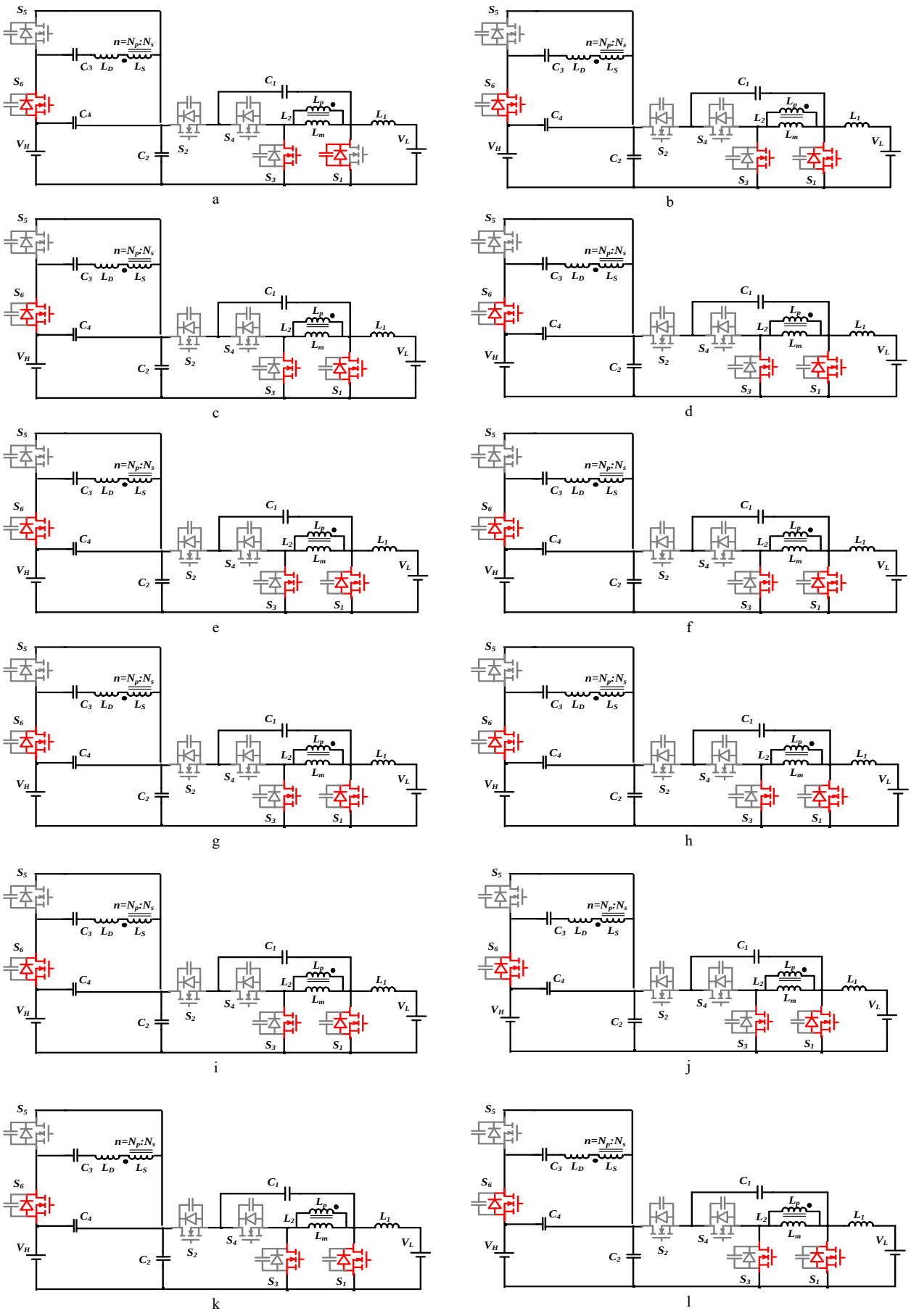


Fig. 2. Equivalent circuit for 12 modes in high step-up operation. (a) Mode 1, (b) Mode 2, (c) S Mode 3, (d) Mode 4, (e) Mode 5, (f) Mode6, (g) Mode 7, (h) Mode 8, (i) S Mode 9, (j) Mode 10, (k) Mode 11, and(l) Mode12

- The voltage ripple of C_1 to C_4, is ignored because they are sufficiently large.
- It is assumed that the elements of converter are ideal, considering only the drain-source capacitances of the MOSFETs in the circuit.
- n is equal to the turn ratio of the coupled inductor, denoted as n = ns/np, and the magnetic coupling K is assumed to be one.
- The capacitors of MOSFETs, C_{ds1} to C_{ds6}, become completely charged and discharged throughout the dead time.
- The diodes connected in parallel to the switches are rapid recovery diodes.

Mode 1 ($t_0<t<t_1$)

This interval starts when switch S_2 is switched off. Since the sum of the initial current of the transformer primary current and capacitor C_1 current is greater than the current i_{L1} (current of input inductor, L_1) at time t_0, the capacitor at drain-source of switch S_1 is initially discharged, after which the body diode under ZVS conditions begins to conduct.

Mode 2 ($t_1<t<t_2$)

When this interval begins, the S_1 switch starts functioning with ZVS situations. As S_6 switch is currently on, the voltage of L_D (V_{LD}) becomes negative, leading to a reduction in the flow of current through it. The formulas for the circuit in mode 2 can be expressed as (1):

$$\begin{cases} V_{Lm} = 0, V_{L1} = V_L, V_{LD} = V_{C3} - V_{C4} \\ I_{C1} = 0, I_{C2} = -I_H, I_{C3} = -I_{LD}, I_{C4} = -I_H + I_{LD} \end{cases} \quad (1)$$

Where I_H denotes the current associated with the voltage of high side (V_H) and V_{Lm} is the voltage of the inductor L_m. Hence, Equation (2) shows the inductor current in state 2.

$$\begin{cases} i_{Lm}(t) = i_{Lm}(t_0) \\ i_{LD} = i_{LD}(t_0) + \dfrac{V_{C3} - V_{C4}}{L_D} t \end{cases} \quad (2)$$

Mode 3 ($t_2<t<t_3$)

When this period begins, switch S_3 has been turned off, and then the body diode of S_4 starts conducting. Under this condition, the voltage of the magnetic inductor Lm becomes negative and not equal to zero. As a result, the Lm current is decreased.

Mode 4 ($t_3<t<t_4$)

Under these situations, Switch S_4 begins to function with ZVS operation. In this period, the voltage of L_D is more negative than in the previous two time frames and nears its minimum value with a steeper slope. In mode 4 the equations related to the circuit are as follows (3):

$$\begin{cases} V_{Lm} = -V_{C1}, V_{L1} = V_L, V_{LD} = -nV_{C1} + V_{C3} - V_{C4} \\ I_{C1} = I_{Lp}, I_{C2} = -I_H, I_{C3} = -I_{LD}, I_{C4} = -I_H + I_{LD} \end{cases} \quad (3)$$

Thus, the equations i_{LD} and i_{Lm} for mode 4 can be represented as (4):

$$\begin{cases} i_{Lm}(t) = i_{Lm}(t_2) - \dfrac{V_{C1}}{L_m} \\ i_{LD} = i_{LD}(t_2) + \dfrac{-nV_{C1} + V_{C3} - V_{C4}}{L_D} t \end{cases} \quad (4)$$

Mode 5 ($t_4<t<t_5$)

This interval starts when the switch S_6 is turned off. First, capacitor C_{ds5} is discharged by current i_{LD} and then the capacitor C_{ds6} starts charging. which causes the diode of switch S_5 to conduct with ZVS situations.

Mode 6 ($t_5<t<t_6$)

Starting from this period, switch S_5 operates with ZVS situation. While the current i_{LD} remains constant, the voltage across inductor L_D is almost zero. The voltage across inductor L_m is likewise negative and, with a slope identical to the prior segment, it attains its lowest value at the conclusion of this segment. The circuit equations in mode 6 can be represented as (5):

$$\begin{cases} V_{Lm} = -V_{C1}, V_{L1} = V_l, V_{LD} = -nV_{C1} + V_{C3} \\ I_{C1} = I_{Lp}, I_{C2} = -I_H, I_{C3} = -I_{LD}, I_{C4} = -I_H \end{cases} \quad (5)$$

So, it can be concluded (6),

$$nV_{C1} = V_{C3} \quad (6)$$

For mode 6, the currents i_{Lm} and i_{LD} can be expressed by the equations given as follows (7):

$$\begin{cases} i_{Lm}(t) = i_{Lm}(t_4) - \dfrac{V_{C1}}{L_m} \\ i_{LD} = i_{LD}(t_4) + \dfrac{-nV_{C1} + V_{C3}}{L_D} t \end{cases} \quad (7)$$

Mode 7 ($t_6<t<t_7$)

Mode 7 begins when the S_4 switch is turned off. The current (I_p), which the drain-source capacitor of switch S_3 is discharged by the current on the primary side of the transformer. and then the body diode of the switch S3 conducts under ZVS situation.

Mode 8 ($t_7<t<t_8$)

During this time, switch S_4 starts operating with ZVS situation. The voltage of L_D becomes positive when switch S_5 is activated, resulting in a rising current flowing through it. The circuit's equations in mode 8 can be represented as (8):

$$\begin{cases} V_{Lm} = 0, V_{L1} = V_L, V_{LD} = V_{C3} \\ I_{C1} = 0, I_{C2} = -I_H, I_{C3} = -I_{LD}, I_{C4} = -I_H \end{cases} \quad (8)$$

Thus, the i_{LD} and i_{Lm} equations for case 8 will be as follows (9):

$$\begin{cases} i_{Lm}(t) = i_{Lm}(t_6) \\ i_{LD} = i_{LD}(t_6) + \dfrac{V_{C3}}{L_D} \end{cases} \quad (9)$$

Mode 9 ($t_8<t<t_9$)

During this time interval, switch S_1 is inactive and due to the active rectification function of switch S_2, the diode on the body of transistor S_2 starts to conduct. In this condition, the voltage of the magnetic inductance L_m becomes positive.

Mode 10 ($t_9<t<t_{10}$)

At this stage, due to the ZVS condition for switch S_2, this switch conducts. At this stage, the L_D voltage increases positively and approaches its peak value with a sharper incline. The circuit equations in mode 10 can be represented as (10):

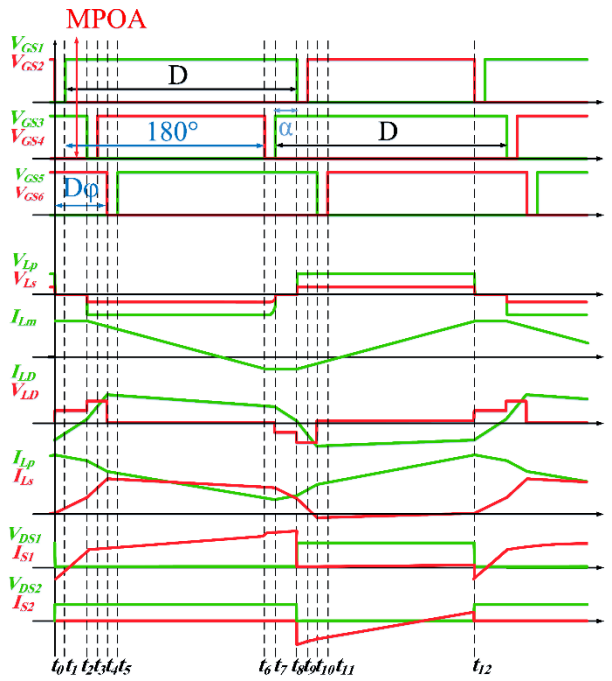


Fig. 3. Theoretical waveforms throughout a switching interval of the suggested converter in step-up operation mode

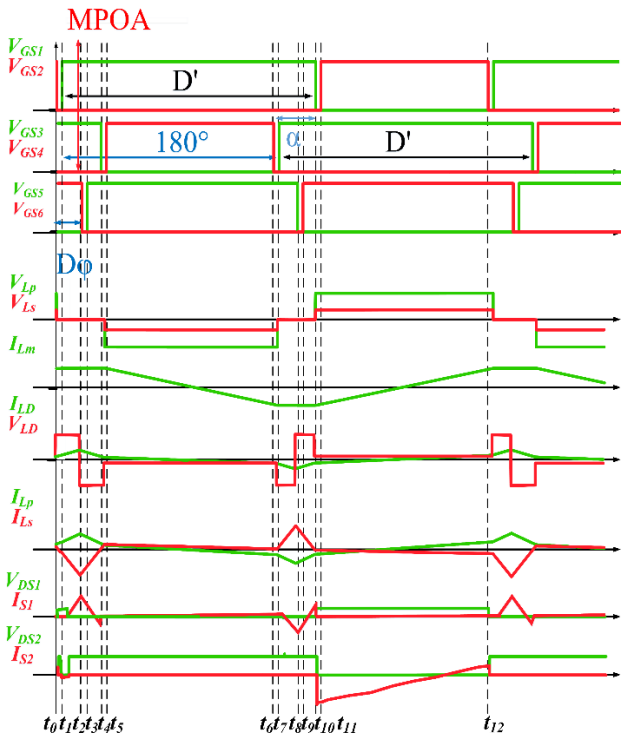


Fig. 4. Theoretical waveforms throughout the switching interval of the proposed converter in step-down operation mode

$$\begin{cases} V_{Lm} = V_{C2} - V_{C1}, V_{L1} = V_L - V_{C2} + V_{C1}, \\ V_{LD} = nV_{C2} - nV_{C1} + V_{C3} \\ I_{C1} = -I_{L1} + I_{Lp}, I_{C2} = -I_H + I_{L1} - I_{Lp} \\ I_{C3} = -I_{LD}, I_{C4} = -I_H \end{cases} \quad (10)$$

The current that flows through the primary winding of the coupled inductor is defined as. Thus, the formulas for i_{LD} and i_{Lm} in mode 10 can be represented as (11):

$$\begin{cases} i_{Lm}(t) = i_{Lm}(t_8) + \dfrac{V_{C2} - V_{C1}}{L_m} \\ i_{LD} = i_{LD}(t_8) + \dfrac{nV_{C2} - nV_{C1} + V_{C3}}{L_D} \end{cases} \quad (11)$$

Mode 11 ($t_{10}<t<t_{11}$)

This time state begins when the S_5 switch is switched off. At first, capacitor C_{ds6} is discharged by current i_{LD}, and subsequently, the diode of S_6 activates under ZVS situation.

Mode 12 ($t_{11}<t<t_{12}$)

In this mode, ZVS conditions are created for switch S_6 so it starts conducting. The L_D voltage is near zero while the i_{LD} current remains constant. The voltage of L_m is above zero, and its current attains its peak value at the conclusion of its ramp, keeping the same slope as the previous mode. The formulas for the circuit in interval 12 represented in this way (12):

$$\begin{cases} V_{Lm} = V_{C2} - V_{C1}, V_{L1} = V_L - V_{C2} + V_{C1}, \\ V_{LD} = nV_{C2} - nV_{C1} + V_{C3} - V_{C4} \\ I_{C1} = -I_{L1} + I_{Lp}, I_{C2} = -I_H + I_{L1} - I_{Lp}, \\ I_{C3} = -I_{LD}, I_{C4} = I_{LD} - I_H \end{cases} \quad (12)$$

Therefore, the equations i_{LD} and i_{Lm} for mode 13 can be expressed as (13):

$$\begin{cases} i_{Lm}(t) = i_{Lm}(t_{10}) + \dfrac{V_{C2} - V_{C1}}{L_m} \\ i_{LD} = i_{LD}(t_{10}) + \dfrac{nV_{C2} - nV_{C1} + V_{C3} - V_{C4}}{L_D} \end{cases} \quad (13)$$

Figs. 2(a-l) and 3 show the operating range and key waveforms of this converter.

It is essential to note that the converter operates in two modes: it functions in step-down mode when $\alpha>D\varphi$ and in step-up mode when $\alpha<D\varphi$, where α signifies the overlap of switches S_3 and S_1, and D denotes the duty cycle of switches S_3 and S_1. It has been mentioned previously that the duty cycle have to be greater than 0.5 to ensure smooth switching of the circuit switches, and $D\varphi$ indicates the time difference between the activation signals for transistors S_5 and S_1. The reference point for phase shift is the duration when S_1 and S_3 operate simultaneously (MPOA, Middle Point of Overlapping Area).

The functioning of a converter in the buck mode is typically akin to the boost mode. To gain a clearer insight into how a step-down mode functions, the theoretical key waveforms associated with it are illustrated in Fig. 4. Additionally, Table I displays the active switches for both modes of step-down and step-up during each interval.

The functioning of a converter in the buck mode is typically akin to the boost mode. To gain a clearer insight into how a step-down mode functions, the theoretical key waveforms associated with it are illustrated in Fig. 4. Additionally, Table I displays the active switches for both modes of step-down and step-up during each interval.

TABLE I
Active Switches During each Interval in Step-up and Step-Down Modes

Time interval	step-up mode	step-down mode
t_0-t_2	$S_1S_3S_6$	$S_1S_3S_6$
t_2-t_4	$S_1S_4S_6$	$S_1S_3S_5$
t_4-t_6	$S_1S_4S_5$	$S_1S_4S_5$
t_6-t_8	$S_1S_3S_5$	$S_1S_3S_5$
t_8-t_{10}	$S_2S_3S_5$	$S_1S_3S_6$
t_{10}-t_{12}	$S_2S_3S_6$	$S_2S_3S_6$

III. Analysis and Design

A. Voltage Gain in Step-Up Modet

Equation (14) shows the voltage on the upper side of the suggested converter. This equation is obtained using the KVL law for the high-side voltage of this converter.

$$V_H = V_{C2} + V_{C4} \tag{14}$$

The voltage gain of the boost converter configuration is obtained as (15) using the volt-second law on the inductors Lm and L_1.

$$\begin{cases} V_{C1} = \dfrac{V_{C2}}{2} \\ \dfrac{V_{C2}}{V_L} = \dfrac{2}{1-D} \end{cases} \tag{15}$$

Equation (16) is obtained by assuming that in the stable condition the voltage of the L_D is approximately zero.

$$\frac{n_s}{n_p} = \frac{V_{C4}}{V_{C2}} = \frac{V_{C4}}{2V_{C1}} = n \tag{16}$$

Equation (17) shows the output voltage gain of the suggested converter operating in boost mode, taking into account equations (14) to (16).

$$G_H = \frac{V_H}{V_L} = \frac{2(n+1)}{1-D} \tag{17}$$

B. Component Design

According to the various modes of the suggested converter, for switches S_1 to S_6, the maximum voltage stress is determined as follows (18):

$$\begin{cases} V_{max,S1} = V_{max,S2} = V_{max,S3} = \dfrac{V_L}{1-D} = \dfrac{V_H}{2(n+1)} \\ V_{max,S4} = \dfrac{2}{1-D} V_L = \dfrac{V_H}{n+1} \\ V_{max,S5} = V_{max,S6} = \dfrac{2n}{1-D} V_L = n\dfrac{V_H}{n+1} \end{cases} \tag{18}$$

The existing stress on the switches can be articulated as (19):

$$\begin{cases} I_{max,S1} = I_{max,S3} = \\ \dfrac{P_{High}}{V_L} + \dfrac{V_L D}{f_s L_1} + \dfrac{V_L D}{2_{Lm}(1-D) f_s} + \dfrac{nV_{C4}}{4L_D f_s}(2D_\varphi - \alpha) \\ I_{max,S2} = I_{max,S4} = \\ \dfrac{nV_{C4}}{4L_D f_s}\alpha + \dfrac{P_{High}}{V_L} + \dfrac{V_L D}{f_s L_1} + \dfrac{V_L D}{2_{Lm}(1-D) f_s} \\ I_{max,S5} = I_{max,S6} = \dfrac{nV_{C4}}{4L_D f_s}(2D_\varphi - \alpha) \end{cases} \tag{19}$$

where f_s is the switching frequency.

Using the value of the inductor current ripple, the value of the inductors can be determined as follows (20):

$$\begin{cases} \Delta i_{L1} = \dfrac{V_L D}{L_1 f_s} \\ \Delta i_{Lm} = \dfrac{V_L D}{L_m f_s (1-D)} \end{cases} \tag{20}$$

The capacitor's voltage can be determined using equations (6), (15), and (16). The potential of the capacitors can be determined from the output voltage as (21).

$$\begin{cases} V_{C1} = \dfrac{V_H}{2(n+1)} \\ V_{C2} = \dfrac{V_H}{n+1} \\ V_{C3} = \dfrac{nV_H}{2(n+1)} \\ V_{C4} = \dfrac{nV_H}{n+1} \end{cases} \tag{21}$$

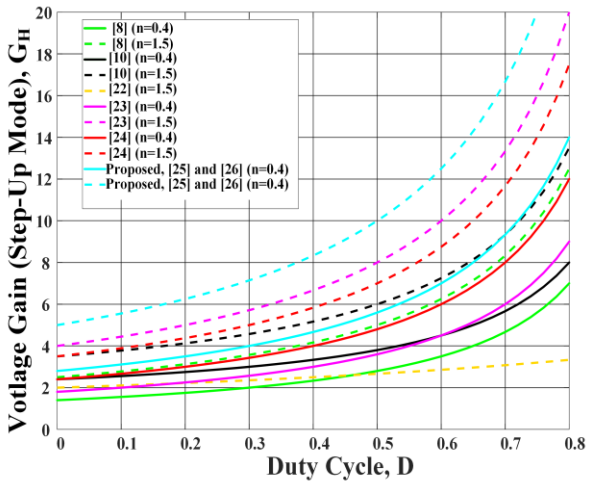
The capacitance of capacitors can be determined by their voltage ripple as (22):

$$\begin{cases} \Delta V_{C1} = \dfrac{2I_{L1}(1-D)}{f_s C_1} \\ \Delta V_{C2} = \dfrac{I_H D}{f_s C_2} \\ \Delta V_{C3} = \dfrac{I_H}{f_s C_3} \\ \Delta V_{C4} = \dfrac{0.5 I_H}{f_s C_4} \end{cases} \tag{22}$$

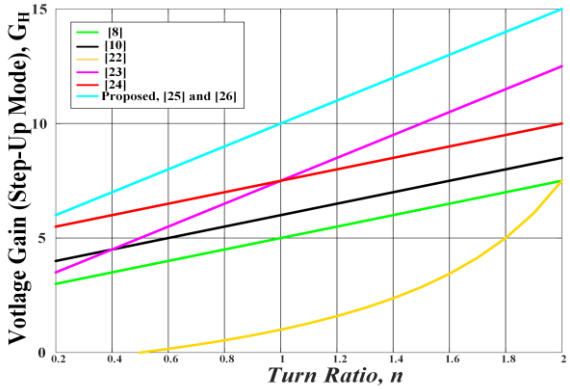
C. Power Transfer Analysis

According to the suggested converter, the conveyed power can be expressed as (23):

$$P_{total} = (V_{C2} + V_{C4}) I_H \tag{23}$$



a



b

Fig. 5. Comparison of voltage gain a versus duty cycle for same turn ratio, and b versus turn ratio for same duty cycle.

To calculate the power component transmitted by the voltage boost cell, middle of current value of switches S_5 and S_6 during one switching cycle should be multiplied by the voltage factor of capacitor C_4 as described in (24):

$$P_{total} = V_{C2} + 3V_{C4}f_s \int_0^{Ts} i_{S5}dt \quad (24)$$

The equations of power for the two operating modes of the suggested converter are obtained after calculating the middle of current of switches S_6 and S_5 with the state equations.

$$For \ \frac{a}{2} < D_\varphi < a$$

$$P_{total} = \frac{V_H^2}{4L_D f_s}\frac{n}{n+1}(\alpha D - 2D_\varphi - \alpha - 2DD_\varphi) \quad (25)$$

and $for \ D_\varphi > a$

$$P_{total} = \frac{V_H^2}{4L_D f_s}\frac{n}{n+1}$$
$$(2D_\varphi - 2DD_\varphi + 4D_\varphi\alpha - \alpha + D\alpha - 2\alpha^2 - 2D_\varphi^2) \quad (26)$$

Equations (23)–(26) show that the transmitted power is affected by the phase shift angle Dφ and the duty cycle D. As the duty cycle is defined by the output and input voltages, the power transfer is regulated by the phase shift. As a result, the converter is capable of functioning with various voltages and power levels.

To ensure ZVS for 6 switches require the inductance Lm must be designed considering the worst-case condition. The condition for ZVS is provided in Equation (27).

$$L_m < \frac{L_D(1-D)}{n\frac{(n+1)}{(1-D)}(A) - n^2(2D_\varphi - \alpha)} \quad (27)$$

$$A = 2D_\varphi - 2DD_\varphi + 4D_\varphi\alpha - \alpha + D\alpha - 2\alpha^2 - 2D_\varphi^2$$

IV. Comparison

This part provides a comparison between the proposed converter and the other BDC converters mentioned in the introduction, as indicated in Table II. In the literature, several methods for DC-DC converters with high step-down/step-up voltage gain are introduced which among them the converters based on coupled inductors are one of the popular approaches to provide high voltage gain. In fact, the topology design approach for BDC converters aimed at achieving a high voltage gain which can be one of the main objectives. Hence, Fig.5 shows the voltage gain comparison of the suggested structure with competing. In the figure, the variations of the voltage amplification in boost configuration are illustrated when the duty cycle and the turn ratio are changed in the range of interest. These variations are plotted in MATLAB. The voltage gain versus duty cycle for the same turn ratio is shown in Fig. 5 (a) while the relationship between voltage gains and turn ratio for a constant duty cycle is shown in Fig. 5 (b). It is evident that the suggested converter offers the ultra gain of voltage when compared to the voltage gains presented in references[8], [10], [22]–[24]. Additionally, it achieves the same voltage level with fewer semiconductor components in comparison to references [25] and [26]. Additionally, the suggested converter offers a higher gain of voltage compared to those in [10] and [21]. The voltage gain of [21] is solely dependent on the duty cycle and the voltage gain of [10] is like [8]. So, the suggested converter offers a significantly higher voltage gain. The details of the specification of the converters are presented in Table II. Also, the suggested converter offers the highest step-down voltage gain compared to others. Furthermore, the suggested converter establishes common ground between the output and input terminals and also has current continuity on the side of low voltage. These features improve converter performance compared to the others. A high voltage gain BDC is suggested based on a reversal coupled inductor in [23]. It is evident that the equation for voltage gain in boost mode includes the turn ratio as a fractional term in the voltage gain formula's denominator. So, it may decrease voltage gain with a high turn ratio and lead to instability with a low turn ratio. As it can be seen, the number of elements of the proposed converter and [24] are almost equal, but the suggested converter offers higher gain of voltage compared to [24]. In [25] a high voltage gain BDC based on coupled inductor and voltage is presented. Likewise observed, the voltage gain is limited compared to the suggested converter and also the input and output currents are discontinuous. The converter proposed by [26] provides the same voltage gain, but the number of semiconductors is higher than the proposed here and the current of the low side is not continuous. Moreover, there is no common ground at input and output terminals in [25] . The proposed converter presented by [26] offers the same voltage gain, but the number of semiconductors is too high. Furthermore, it uses two coupled inductors to provide high voltage gain.

The comparison table illustrates the total voltage stress on semiconductor elements in the proposed converter compared

to others. As can be seen, the proposed converter experiences lower voltage stress than converters with the same voltage gains, resulting in reduced costs and increased efficiency. Moreover, the overall voltage stress on switches.

exhibits only a marginal difference compared to converters with a minor voltage gain, while the gain of voltage is significantly higher. In addition, the suggested converter provides interleaved capabilities that can diminish enhance power quality and the input current ripple.

V. Experimental Results

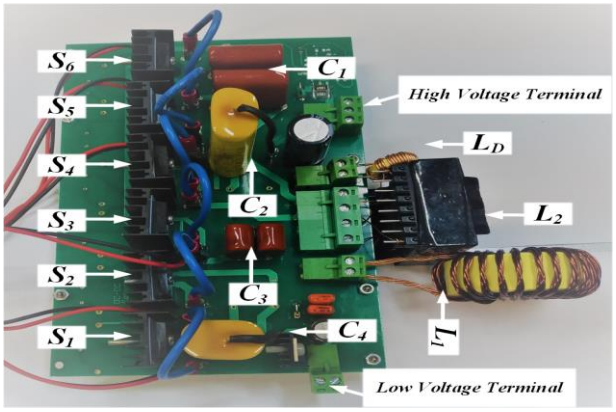
In this section, the experimental results are presented. Before conducting an experimental assessment of the converter's performance, it was initially simulated using PSIM software. Subsequently, a laboratory setup was constructed and utilized to verify the operational and analytical findings of the suggested converter. The conditions and parameters of the converter for testing are provided in Table III. The prototype for the BDC is depicted in Fig. 6. The results of the experiment are presented for boost mode. Thus, input voltages of 50 V DC and output voltage of 300 V DC are considered, a value frequently utilized in industries like single-phase inverters and electric vehicles. Notably, different input and output voltages can be obtained by altering the design through the use of equations (14)-(26).

The EE42 ferrite core is encased by the coupled inductor, whereas the L_D and input inductors are wrapped around toroidal cores. (Due to its efficiency, accessibility, and affordability) That features an air gap in its legs. A controller board utilizing the STM32F303RBT microcontroller and TLP350 gate drivers generates PWM signals in a loop control system. (to evaluate the performance and operational modes of the converter). Fig. 6(b) displays the control board. The control board consists of three parts: the flyback power supply, the microcontroller, and the gate drivers. For generating gate signals, the microcontroller provides three PWM channels. The circuits for the gate driver consist of six TLP350.

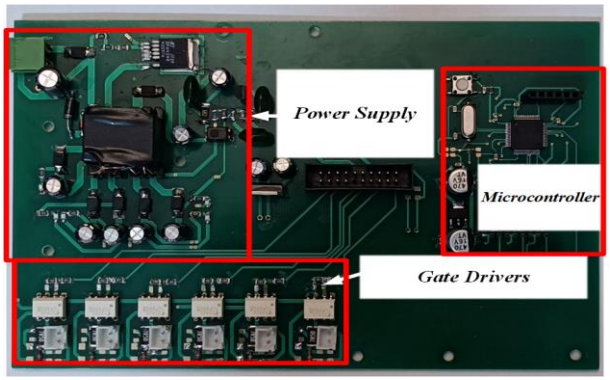
Fig. 7 presents the experimental findings for the buck and boost configurations. The stable waveforms of Fig. 7(a) show the current and input/output voltages of the proposed converter. The input voltage (V_{Low}) is 50V DC in the step-up mode, while the high-side voltage (V_{High}) is maintained at 301.2V DC. The efficiency measured at the nominal output power, is 96.23%. Fig. 7(b) show the voltage of capacitors C_1 to C_4. The signals produced by gate drivers are illustrated in Fig. 7(c). The gate signal of S_3 (V_{gs3}) is 180 degrees behind the gate signal of S_1 (V_{gs1}). The signal of gates for switches S_1, S_3, and S_5 are opposite to those of switches S_2, S_4, and S_6. Fig. 7(d) show the voltage of the switches S_1 and S_2 (V_{DS1} and Fig. 7 presents the experimental findings for the buck and boost configurations. The stable waveforms of Fig. 7(a) show the current and input/output voltages of the proposed converter. The input voltage (V_{Low}) is 50V DC in the step-up mode, while the high-side voltage (V_{High}) is maintained at 301.2V DC. The efficiency measured at the nominal output power, is 96.23%. Fig. 7(b) show the voltage of capacitors C_1 to C_4. The signals produced by gate drivers are illustrated in Fig. 7(c). The gate signal of S_3 (V_{gs3}) is 180 degrees behind the gate signal of S_1 (V_{gs1}). The signal of gates for switches S_1, S_3, and S_5 are opposite to those of switches S_2, S_4, and S_6. Fig. 7(d) show the voltage of the switches S_1 and S_2 (V_{DS1} and V_{DS2}).

TABLE II
Comparison Among Various BDC

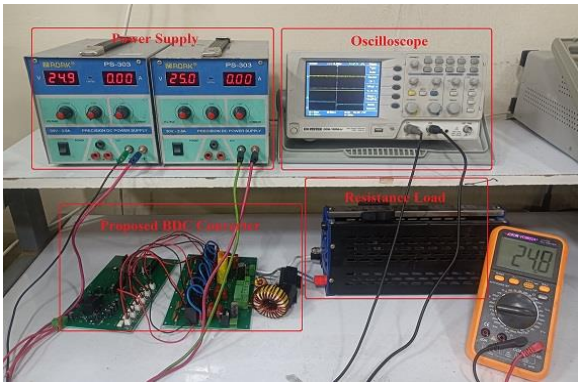
Feature	Proposed Converter	[26]	[25]	[24]	[23]	[22]	[10]	[8]
No. of semiconductors	6	8	7	4	6	4	4	4
No. of inductors	2	-	-	-	2	-	-	-
No. of coupled inductor	1	2	2	1	1	1	1	1
No. of capacitors	4	4	3	2	3	2	2	3
Voltage gain (boost mode)	$\frac{2(n+1)}{1-D}$	$\frac{2(n+1)}{1-D}$	$\frac{2(n+1)}{1-D}$	$\frac{n+2}{1-D}$	$\frac{2n+1}{1-D}$	$\frac{2n-1}{(n-1)(1-D)}$	$\frac{2+n-D}{1-D}$	$\frac{n+1}{1-D}$
Voltage gain (buck mode)	$\frac{D'}{2(n+1)}$	$\frac{D'}{2(n+1)}$	$\frac{D'}{2(n+1)}$	$\frac{D'}{n+2}$	$\frac{D'}{2n+1}$	$\frac{(n+1)D'}{2n-1}$	$\frac{D'}{1+n+D'}$	$\frac{D'}{n+1}$
Total voltage stress across semiconductors/ V_H	$\frac{4n+5}{2n+2}$	$\frac{6n+5}{2n+2}$	$\frac{6n+8}{2n+2}$	2	$\frac{4n+4}{2n+1}$	2	2	$2+\frac{2n}{1-D}$
Reported efficiency at nominal power in boost mode (%)	96.23	94.9	96.3	96	97	95.22	97	95.2
Continuous input current at low voltage side	Yes	Yes	No	No	Yes	No	No	No
Common ground between input/output	Yes	Yes	No	No	Yes	Yes	Yes	Yes



a



b



c

Fig. 6. Experimental prototype, a power converter, b gate drivers and microcontroller, c experimental setup.

The voltage stress for these switches is identical to that determined in equation (18). The waveforms corresponding to the voltages of switches S_3, S_4, and S_6 are shown in Fig. 7(e) displays the voltage waveforms for switches S_3, S_4, and S_6.

Fig. 7 (f) show the waveforms of voltage and current for both the primary and secondary of the coupled inductor. The voltage waveforms for the primary and secondary are represented as V_{Lp} and V_{Ls}, respectively. The currents in the primary and secondary windings of the coupled L_2, are represented as I_{Lp} and I_{Ls}, respectively. Different waveforms of multiple components of the proposed converter are shown to confirm the performance of the converter. To verify the ZVS functioning of the converter, the enlarged view of the waveforms is shown in Figs 7(g)-(i). The voltage, current, and input gate for switches S_1 and S_3 are illustrated in Fig. 7 (g) and (h).

TABLE III
Experimental Condition and Parameters

Parameters	Value
P_o ,Output power	350 W
V_{High} ,High voltage	300 V_{dc}
V_{Low} ,Low voltage	50 V_{dc}
f_s ,Switching frequency	50 kHz
L_D *and* L_{in} ,Inductors	47µH ,100µH
L_m ,Coupled Inductor, , turn ratio	250µH, 0.37
C_1, C_2, C_3 & C_4,capacitors	10µF, 12µF. 10µF, 12µF
S_1, S_2 & S_3,Switches	IRFP260NPBF
S_4,Switch	IPW60R060P7
S_5 & S_6,Switches	IRFP150NPB

Fig. 7(i) additionally presents findings for the input gate and voltage of switch S_5. Additionally, the waveform of the magnetizing current for the coupled inductor is displayed in Fig. 7(i). It is evident that zero-voltage switching is available for the switches. Thus, the power loss is reduced, and the switch activates under soft switching conditions. Fig. 8 shows the outcomes for buck mode functionality. Fig. 7(j) shows the signal gates of switches S1, S_3, and S_5. The signal gates of switches S_2, S_4, and S_6 are opposite to those of switches S_1, S_3, and S_5. The input voltage for buck operation is 300V, producing an output voltage of 49.87V. Fig. 7(k) illustrates the voltage across the capacitors, whereas Fig. 7(l) represents the voltage across switches S_1, S_3, and S_5. The outcomes for buck mode indicate that the converter delivers strong performance across various components.

The distribution of power loss is determined using the RMS current, current and voltage waveforms, peak voltage, along with the switching frequency. Fig. 8 illustrates the efficiency results for various load conditions. For load levels between 80% and nominal power, the efficiency is greater than 96%.

Consequently, the experimental results validate the effective operation of the suggested converter, demonstrating its appropriateness for multiple applications. The result of experimental confirm the efficient operation of the suggested converter, demonstrating its appropriateness for multiple applications.

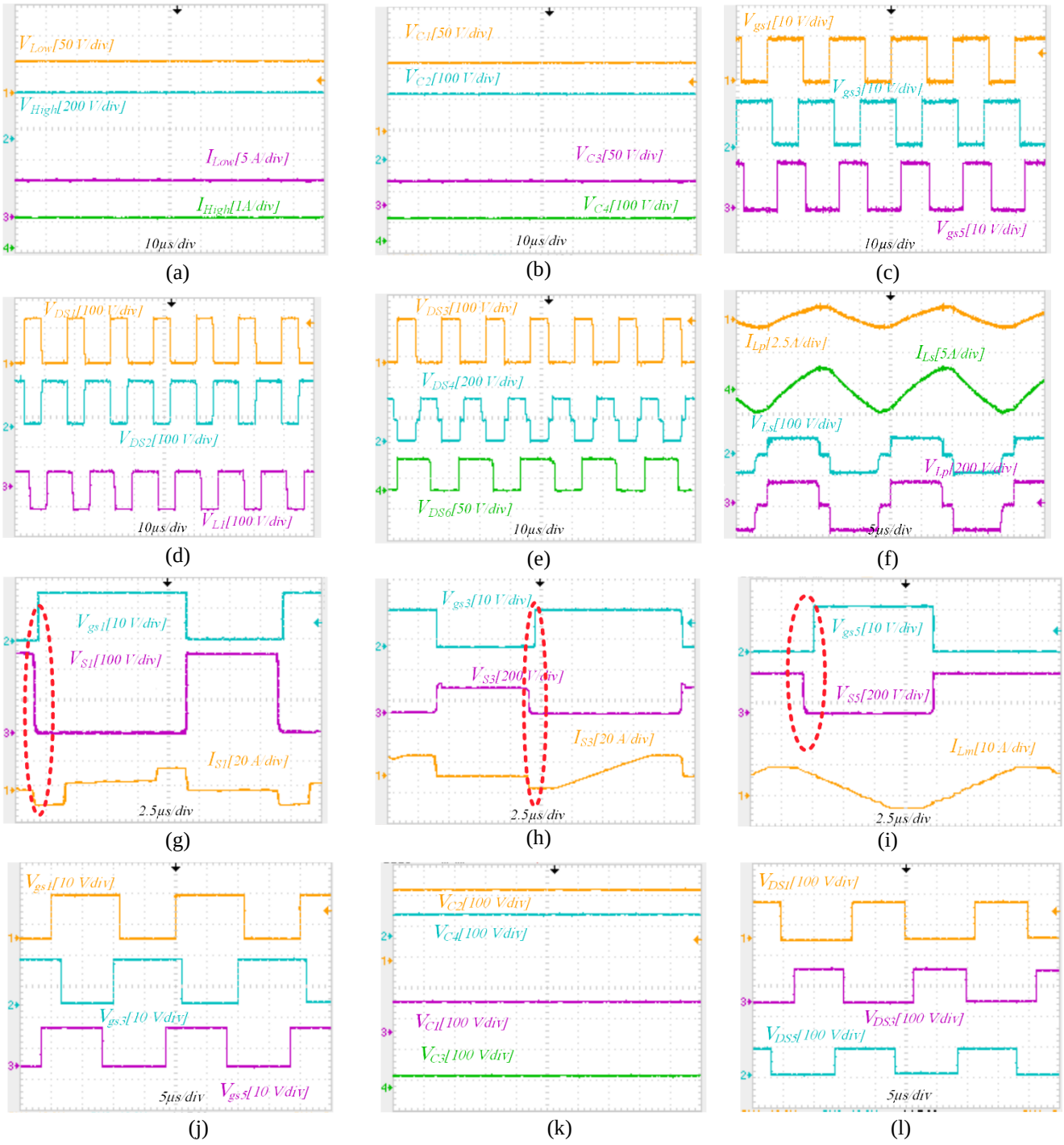


Fig. 7. Experimental data includes (a) waveforms for input and output, (b) voltages of capacitors, and (c) input gate measurements for switches S1, S3, and S5, (d) the voltage across S1 and S2, along with the voltage across the input inductor, (e) voltages of S3, S4, and S6, (f) voltage and current waveforms for the coupled inductor, (g) a detailed view of the input gate, voltage, and current for switch S1, (h) a detailed view of the input gate, voltage, and current for switch S3, and (i) a detailed view of the input gate, voltage for switch S5, and the magnetizing current for the coupled inductor. Additionally, (j) input gate data for switches S1, S3, and S5, (k) voltages across capacitors, and (l) voltages of switches S1, S3, and S5

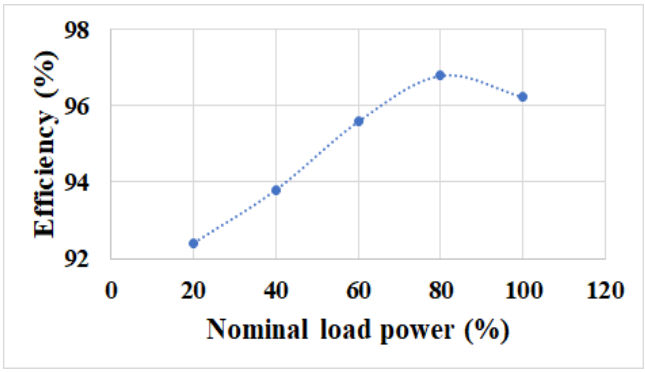


Fig. 8. The efficiency curve as a function of nominal power.

VI. Conclusion

This paper presented an innovative power converter featuring a high voltage gain BDC through the use of a Asymetrical Voltage Multiplayer cell, a coupled inductor, and two-phase boost converter. Various switching modes of the converter are examined, and equations for each mode are presented. Additionally, the design equations for various elements are outlined. The suggested converter offers the greatest voltage gain in comparison to many competitors and contains fewer components than other converters with equivalent voltage gain. Additionally, it provides a steady

current on the low voltage side. ZVS switching is implemented, enhancing the efficiency of the converter. Using an asymmetrical design of the voltage multiplier cell can reduce total losses due to the voltage distribution strategy and reduced peak currents. The experimental findings indicate that the converter's performance is satisfactory and that it can deliver a high voltage from a low voltage according to pre-defined specifications.

ACKNOWLEDGMENT

The authors acknowledge Semnan University.

FUNDING STATEMENT

This research received no specific grant from any funding agency in the public, commercial, or not-for-profit sectors.

CONFLICTS OF INTEREST

The second author is a Director-in-Charge for Modeling and Simulation in Electrical and Electronics Engineering Journal and was not involved in the editorial review or the decision to publish this article.

AUTHOR'S CONTRIBUTION STATEMENT

Conceptualization and study design: (Madai, Molla-Ahmadian)
Data collection and experimentation: (Madai, Jazaeri, Molla-Ahmadian)
Data analysis and interpretation: (Madai, Jazaeri, Molla-Ahmadian)
Manuscript writing and editing: (Madai, Jazaeri, Molla-Ahmadian)
Supervision and project administration: (Jazaeri, Molla-Ahmadian)

AI DISCLOSURE

AI was used only as a tool for language editing.

REFERENCES

[1] M. Babaei, S. Sharifi, and M. Monfared, “A Z-source network integrated buck–boost PFC rectifier,” Int. J. Ind. Electron., Control Optim., vol. 2, no. 2, pp. 289–296, Oct. 2019, doi: 10.22111/ieco.2018.26296.1073.

[2] K. Varesi and S. Padmanaban, “A transformer-less high-boosting common-grounded multi-phase DC–DC converter with continuous input-current favourable for low-power applications,” IET Renew. Power Gener., vol. 16, no. 3, pp. 594–604, Mar. 2022, doi: 10.1049/rpg2.12591.

[3] S. O. Golpayegani, M. Jazaeri, and N. Eskandarian, “Frequency domain analysis of dual active bridge converter considering all power loss elements,” J. Model. Simul. Electr. Electron. Eng., vol. 3, no. 2, pp. 45–56, Aug. 2023, doi: 10.22075/mseee.2024.33381.1149.

[4] M. Elmi, M. Banaei, and H. Afsharirad, “Study on a non-isolated high step-up SEPIC-based DC–DC converter with continuous input current for photovoltaic applications,” Int. J. Ind. Electron., Control Optim., vol. 3, no. 1, pp. 95–104, Mar. 2025, doi: 10.22111/ieco.2024.48587.1558.

[5] W. Li, X. He, D. Xu, and B. Wu, “General derivation law of nonisolated high-step-up interleaved converters with built-in transformer,” IEEE Trans. Ind. Electron., vol. 59, no. 3, pp. 1650–1661, Mar. 2012, doi: 10.1109/TIE.2011.2163375.

[6] A. Rodriguez, A. Vazquez, D. G. Lamar, M. M. Hernando, and J. Sebastian, “Different purpose design strategies and techniques to improve the performance of a dual active bridge with phase-shift control,” IEEE Trans. Power Electron., vol. 30, no. 2, pp. 790–804, Feb. 2015, doi: 10.1109/TPEL.2014.2309853.

[7] S. Zong, H. Luo, W. Li, Y. Deng, and X. He, “High-power bidirectional resonant DC–DC converter with equivalent switching frequency doubler,” IET Renew. Power Gener., vol. 10, no. 6, pp. 834–842, Jul. 2016, doi: 10.1049/iet-rpg.2015.0437.

[8] J. Hiltunen, V. Vaisanen, R. Juntunen, and P. Silventoinen, “Variable-frequency phase shift modulation of a dual active bridge converter,” IEEE Trans. Power Electron., vol. 30, no. 12, pp. 7138–7148, Dec. 2015, doi: 10.1109/TPEL.2015.2390913.

[9] M. Packnezhad, P. Talebi, and H. Farzanehfard, “Fully soft-switched high step-up/down bidirectional buck/boost converter with reduced switch voltage stress,” IET Power Electron., vol. 16, no. 1, pp. 105–115, Jan. 2023, doi: 10.1049/pel2.12457.

[10] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, “Step-up DC–DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications,” IEEE Trans. Power Electron., vol. 32, no. 12, pp. 9143–9178, Dec. 2017, doi: 10.1109/TPEL.2017.2652318.

[11] H. Wu, K. Sun, L. Chen, L. Zhu, and Y. Xing, “High step-up/step-down soft-switching bidirectional DC–DC converter with coupled-inductor and voltage matching control for energy storage systems,” IEEE Trans. Ind. Electron., vol. 63, no. 5, pp. 2892–2903, May 2016, doi: 10.1109/TIE.2016.2517063.

[12] K. Filsoof and P. W. Lehn, “A bidirectional modular multilevel DC–DC converter of triangular structure,” IEEE Trans. Power Electron., vol. 30, no. 1, pp. 54–64, Jan. 2015, doi: 10.1109/TPEL.2014.2307004.

[13] C. Pineda, J. Pereda, F. Rojas, C. Cerda, X. Zhang, and A. J. Watson, “Asymmetrical triangular current mode (ATCM) for bidirectional high step ratio modular multilevel DC–DC converter,” IEEE Trans. Power Electron., vol. 35, no. 7, pp. 6906–6915, Jul. 2020, doi: 10.1109/TPEL.2019.2957951.

[14] C. Pineda, J. Pereda, F. Rojas, G. Droguett, C. Burgos-Mellado, and A. J. Watson, “Optimal ZCS modulation for bidirectional high-step-ratio modular multilevel DC–DC converter,” IEEE Trans. Power Electron., vol. 36, no. 11, pp. 12540–12550, Nov. 2021, doi: 10.1109/TPEL.2021.3078235.

[15] S. T. S. Lee, S. Y. R. Hui, W. C. Chow, and H. S. H. Chung, “Development of a switched-capacitor DC–DC converter with bidirectional power flow,” IEEE Trans. Circuits Syst. I Fundam. Theory Appl., vol. 47, no. 9, pp. 1383–1389, Sep. 2000, doi: 10.1109/81.883334.

[16] H. Shayeghi, S. Pourjafar, and S. M. Hashemzadeh, “A switching capacitor based multi-port bidirectional DC–DC converter,” IET Power Electron., vol. 14, no. 9, pp. 1622–1636, Sep. 2021, doi: 10.1049/pel2.12137.

[17] R. Hu, J. Zeng, J. Liu, and K. W. E. Cheng, “A nonisolated bidirectional DC–DC converter with high voltage conversion ratio based on coupled inductor and switched capacitor,” IEEE Trans. Ind. Electron., vol. 68, no. 2, pp. 1155–1165, Feb. 2021, doi: 10.1109/TIE.2020.2967667.

[18] S. A. Gorji, H. G. Sahebi, M. Ektesabi, and A. B. Rad, “Topologies and control schemes of bidirectional DC–DC power converters: An overview,” IEEE Access, vol. 7, pp. 117997–118019, Aug. 2019, doi: 10.1109/ACCESS.2019.2937239.

[19] H. Ardi, A. Ajami, F. Kardan, and S. N. Avilagh, "Analysis and implementation of a nonisolated bidirectional DC–DC converter with high voltage gain," IEEE Trans. Ind. Electron., vol. 63, no. 8, pp. 4878–4888, Aug. 2016, doi: 10.1109/TIE.2016.2552139.

[20] H. S. Lee and J. J. Yun, "High-efficiency bidirectional buck–boost converter for photovoltaic and energy storage systems in a smart grid," IEEE Trans. Power Electron., vol. 34, no. 5, pp. 4316–4328, May 2019, doi: 10.1109/TPEL.2018.2860059.

[21] N. A. Dung, H.-J. Chiu, Y.-C. Liu, and P. J. Huang, "Analysis and implementation of a high voltage gain 1 MHz bidirectional DC–DC converter," IEEE Trans. Ind. Electron., vol. 67, no. 2, pp. 1415–1424, Feb. 2020, doi: 10.1109/TIE.2019.2905810.

[22] V. V. S. K. Bhajana, P. Drabek, M. Jara, M. Popuri, A. Iqbal, and C. B. B., "Investigation of a bidirectional DC–DC converter with zero-voltage switching operation for battery interfaces," IET Power Electron., vol. 14, no. 3, pp. 614–625, Mar. 2021, doi: 10.1049/pel2.12048.

[23] H. Liu, L. Wang, Y. Ji, and F. Li, "A novel reversal coupled inductor high-conversion-ratio bidirectional DC–DC converter," IEEE Trans. Power Electron., vol. 33, no. 6, pp. 4968–4979, Jun. 2018, doi: 10.1109/TPEL.2017.2725358.

[24] H. Bahrami, S. Farhangi, H. Iman-Eini, and E. Adib, "Analysis, design, and implementation of DC–DC IBBC–DAHB converter with voltage matching to improve efficiency," IEEE Trans. Ind. Electron., vol. 66, no. 7, pp. 5209–5219, Jul. 2019, doi: 10.1109/TIE.2018.2868260.

[25] Z. Hosseinzadeh, N. Molavi, and H. Farzanehfard, "Soft-switching high step-up/down bidirectional DC–DC converter," IEEE Trans. Ind. Electron., vol. 66, no. 6, pp. 4379–4386, Jun. 2019, doi: 10.1109/TIE.2018.2863216.

[26] M. R. Mohammadi, A. Amoorezaei, S. A. Khajehoddin, and K. Moez, "A high step-up/step-down LVS-parallel HVS-series ZVS bidirectional converter with coupled inductors," IEEE Trans. Power Electron., vol. 37, no. 2, pp. 1945–1961, Feb. 2022, doi: 10.1109/TPEL.2021.3106668.

[27] R. Hu, H. Qi, Z. Yan, W. Wu, J. Zeng, and J. Liu, "A coupled-inductor-based bidirectional DC–DC converter with high voltage conversion ratio and sensorless current balance," IEEE Trans. Ind. Electron., vol. 70, no. 3, pp. 2450–2460, Mar. 2023, doi: 10.1109/TIE.2022.3172770.

[28] M. Madadi, M. Jazaeri, and H. Molla-Ahmadian, "Design and implementation of an ultra-high gain, soft-switching, bidirectional DC–DC converter with high efficiency," e-Prime – Adv. Electr. Eng., Electron. Energy, vol. 12, pp. 101002, Jun. 2025, doi: 10.1016/j.prime.2025.101002.

[29] E. Babaei, Z. Saadatizadeh, and C. Cecati, "High step-up high step-down bidirectional DC–DC converter," IET Power Electron., vol. 10, no. 12, pp. 1556–1571, Dec. 2017, doi: 10.1049/iet-pel.2016.0977.

[30] M. Babaei and M. Monfared, "High step-down bridgeless SEPIC/Cuk PFC rectifiers with improved efficiency and reduced current stress," IEEE Trans. Ind. Electron., vol. 69, no. 10, pp. 9984–9991, Oct. 2022, doi: 10.1109/TIE.2022.3159954.

[31] D. Graovac and M. Pürschel, "MOSFET power losses calculation using the data-sheet parameters," Infineon Technologies AG, Munich, Germany, Appl. Note AN-201, Jan. 2006.

[32] A. H. Masoumi, S. Sharifi, M. Monfared, and S. Karbasforooshan, "Γ-source magnetic integrated filter for single-phase grid tied voltage source converters," IEEE Trans. Ind. Electron., early access, 2019, doi: 10.1109/TIE.2019.2934031.

[33] R. W. Erickson and D. Maksimović, Fundamentals of Power Electronics, 3rd ed. Cham, Switzerland: Springer, 2020, doi: 10.1007/978-3-030-43881-4.

BIOGRAPHIES

Mahdi Madadi received the B.Sc. degree in electronic engineering from Shahid Rajaee University, Tehran, Iran, in 2005, and M.Sc. degree in electrical engineering from the Islamic Azad University, Science and Research Branch, Tehran, Iran, in 2014. He is currently a PhD student in the department of electrical engineering at Semnan University. His research interests include the design and modeling of power converters and renewable energy systems.

Mostafa Jazaeri received the B.Sc. degree from Sharif University of Tech., Tehran, Iran in 1986, the M.Sc. degree from Ferdowsi University of Mashhad, Mashhad, Iran in 1992 and the Ph.D. degree from University of Bath, Bath, UK, in 2003 all in electrical engineering. He is currently an associate Prof. with the department of electrical and computer engineering, Semnan University. His main research interests include power system dynamics and control, AC/DC systems, FACTS.

Hamed Molla-Ahmadian received the B.S. degree in electrical engineering from the Ferdowsi University, Mashhad, Iran, in 2004, the M.Sc. degree in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 2007, and the Ph.D. degree in electrical engineering from Ferdowsi University, Mashhad in 2012. In 2007, he joined Khorasan Institute of Higher Education, Mashhad, Iran, where he is currently an Assistant Professor. Since 2008, he has been the Entrepreneur and the Chairman of Tajhizat Abzarazma Co, Mashhad, Iran. His research interests include the hybrid and switched systems, modeling and control of power electronic converters, and electronic measurement.