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A Novel Method for Inverter Fault Localization in CSC-HVDC System Using DC Current Component

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Abstract **-- Internal faults within the current source converter–based high-voltage direct current (CSC-HVDC) systems pose serious threats to system reliability and operational security. While integrated protection and control schemes can effectively clear most temporary faults, permanent faults or failures in the control system require accurate localization to enable targeted isolation procedures. Moreover, recurrent transient faults demand timely diagnostic interventions to prevent equipment degradation. This paper focuses on short circuit faults that occur within the inverter stage of CSC-HVDC systems. Considering the converter control dynamics, arm currents are monitored under both forced-alpha operation and normal operating conditions. A novel diagnostic approach is proposed, in which the DC current component is exploited as a distinctive signature to achieve precise arm-level fault localization. The method is computationally simple, does not require high sampling rates, and identifies the fault location within a maximum of two cycles, allowing for isolation before forced-alpha mode is activated. The proposed technique is validated through detailed simulations of the Hydro-Quebec monopolar CSC-HVDC test system in MATLAB/Simulink, demonstrating its effectiveness and rapid response under various fault scenarios.**

Index Terms**: Current Source Converter, High Voltage Direct Current System, Inverter Fault, 12-pulses Converter.**

I. INTRODUCTION

TODAY, high voltage direct current (HVDC) systems are increasingly favored for power transmission, offering three key advantages over high voltage alternating current (HVAC) systems: (1) more economical long-distance power transfer, (2) enhanced controllability and stability, and (3) asynchronous network interconnection capability [1]. Due to the massive amount of energy transmitted by the HVDC system, the reliability and security of this system have a direct impact on the security and stability of the entire system [2]. Consequently, HVDC protection systems have become a critical area of research focus in power systems.

HVDC systems experience multiple fault types, including alternating current (AC) system faults, converter internal faults, and direct current (DC) system faults. The main reason for these faults is insulation failure due to short circuit, lightning, or switching [3]. Extensive research has been conducted on internal faults in converters, with the most prevalent protection schemes being differential protection, overcurrent protection, and direct digital protection [4]-[6]. Due to the high cost and complexity of control associated with direct digital protection, converter switch protection primarily relies on differential and overcurrent relays [7].

A significant challenge during asymmetrical faults in thyristor legs is the generation of inrush current in the converter transformer. This phenomenon can lead to maloperation or even system failure, as conventional differential protection often responds too slowly. To mitigate this risk, faster alternative protection methods must be implemented [8]. The DC blocking method is a protection scheme used to detect and isolate internal short circuit faults

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in converters, effectively containing fault propagation to adjacent AC/DC subsystems while maintaining grid stability. This approach provides faster fault clearance than conventional differential protection, typically isolating the affected converter within 2-5 ms to prevent cascade failures in the interconnected power system [9]. Modern protection schemes should implement a multi-level blocking strategy to maintain system availability during fault isolation [10].

Another approach for fault location detection in converters involves analyzing the circuit state characteristics and measuring the time differences between signals at different converter terminals. This method enables precise determination of both the fault location and fault type [11]. This technique is commonly employed in modular multilevel converter (MMC) systems, where it facilitates real-time monitoring of individual submodule voltages to enable precise fault detection and localization. Additionally, fault zone identification can be achieved by monitoring transient phenomena and analyzing voltage waveform characteristics across predefined converter sections, enabling precise localization of the faulted area [12], [13]. This method requires a high sampling rate (>1000 kHz) and employs wavelet transform techniques, making it effective in MMC-based HVDC systems.

Given the advancements in signal processing techniques in recent years, a method for detecting faults within the converter can be proposed using either the wavelet transform or the Stockwell transform [14], [15]. In the wavelet transform method, selecting the appropriate mother wavelet is crucial for both the accuracy and speed of fault detection. Additionally, this method is susceptible to noise, and the presence of electromagnetic interference in the current source converter (CSC) can distort the wavelet coefficients. On the other hand, the Stockwell transform method, which combines wavelet and Fourier transforms for fault detection, comes with a high computational cost. Moreover, interpreting its results typically requires advanced classification algorithms.

Additionally, these two methods may fail to accurately distinguish between internal converter faults and DC-side faults, load variations, or AC grid disturbances.

Modern HVDC protection systems are increasingly employing intelligent techniques such as artificial neural networks (ANNs) and support vector machines (SVMs) for fault detection, thereby enhancing the reliability and performance of conventional protection schemes. [16], [17]. Neural networks, being more straightforward to implement, are primarily employed for preliminary detection of basic faults and demonstrate moderate accuracy in complex fault scenarios. The SVM approach shows strong performance with limited datasets but faces challenges when handling large-scale data, and is predominantly utilized for fault classification. A key limitation of these intelligent methods is their substantial requirement for training data. This poses practical challenges for HVDC systems, as acquiring real-world internal converter fault data is both technically difficult and economically costly.

The unique configuration of controlled thyristor arms in CSCs and the specific control characteristics of CSC-HVDC systems enable partial implementation of both DC protection and inverter protection during commutation faults. Numerous studies have demonstrated that these protection systems can achieve satisfactory performance when coordinated adequately with the converter's control strategy. In the event of a permanent fault or failure of the control system, we require an effective protection structure to identify the most detailed part of the fault as possible and to minimize stress on the equipment and system through appropriate protective operations, such as repair or replacement of the faulty part.

In this paper, the effect of control parameters in various fault conditions within the inverter is investigated, and a protection structure is presented that can determine the fault arm in the event of control system failure or the presence of a permanent fault. This method utilizes a comparison of DC versus arm current to detect the faulty arm prior to forced alpha function activation, enabling preemptive isolation of the faulted section and maintaining uninterrupted system operation. The main contributions of this paper are summarized as follows:

- A novel DC-current-signature-based algorithm for arm-level fault localization in CSC inverters.
- Demonstration of fault identification within two cycles using low-rate sampling and a simple decision rule.
- Validation on the Hydro-Quebec monopolar CSC-HVDC test system simulated in MATLAB/Simulink across a range of permanent and transient fault scenarios, including cases with control-system failures and commutation disturbances.

The different sections of the article are as follows:

In Section 2, the structure of the system under study is examined. In Section 3, the control characteristic diagram and the control modes of the system are described. In Section 4, various permanent and transient faults on the thyristor arms of the inverter are simulated, and the performance of the control system for fault suppression is examined. In Section 5, a protection method is presented that can detect the location of the fault inside the converter, based on the presence of the DC component in the thyristor arms.

II. The Studied Network

The system analyzed in this paper is derived from Hydro-Quebec monopolar HVDC link. It transmits 1000 MW at ±500 kV DC and 2 kA via a 300 km DC line, interconnecting a 5000 MW, 500 kV, 60 Hz AC grid (rectifier) with a 10,000 MW, 345 kV, 50 Hz AC grid (inverter). Both rectifier and inverter utilize twelve-pulse thyristor-based CSCs, which significantly reduce harmonic distortion in both DC voltage and current, as well as in AC waveforms, compared to six-pulse converters. According to Fig. 1, the converters are connected to the AC system through a three-winding Y/Y/Δ transformer and to the DC system through a 0.5 H smoothing inductor. The AC filters installed on the AC side of both converters prevent the odd harmonics of the current from entering the AC system and act as a large capacitor at the fundamental frequency, compensating for the reactive power consumed by the rectifier due to the firing angle α. The DC filters also prevent the voltage harmonics from entering the DC system.

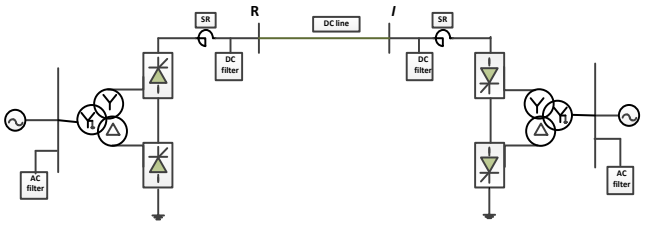

Fig. 1. Monopolar HVDC network with CSC.

Fig. 2 illustrates the internal structure of a twelve-pulse CSC. Each twelve-pulse converter comprises two six-pulse converters supplied via a three-winding transformer with star and delta connections. The converter connected to the star connection of the transformer is referred to as a star converter. In contrast, the converter connected to the delta connection of the transformer is referred to as a delta converter.

According to Fig. 2, each converter contains two upper and lower legs, with each leg comprising three arms. Within every arm, thousands of thyristors are connected in series. This article aims to investigate and precisely locate faults occurring within individual arms of this configuration.

Throughout this article, the following nomenclature applies with reference to Fig. 2: S denotes the star converter, D denotes the delta converter, U and L represent the upper and lower legs, respectively, and numerals 1 through 3 identify the arm positions. For example, SU1 indicates the first arm at the upper leg of the star converter. Since the current source is supplied from the DC line side, current measurements are positioned at the upper terminal of each arm, denoted as 'M' in Fig. 2. In this article, we investigate internal faults within the converter arms—exemplified by the SU1 fault location marked 'F' in Fig. 2—and develop an algorithm to identify such fault positions precisely.

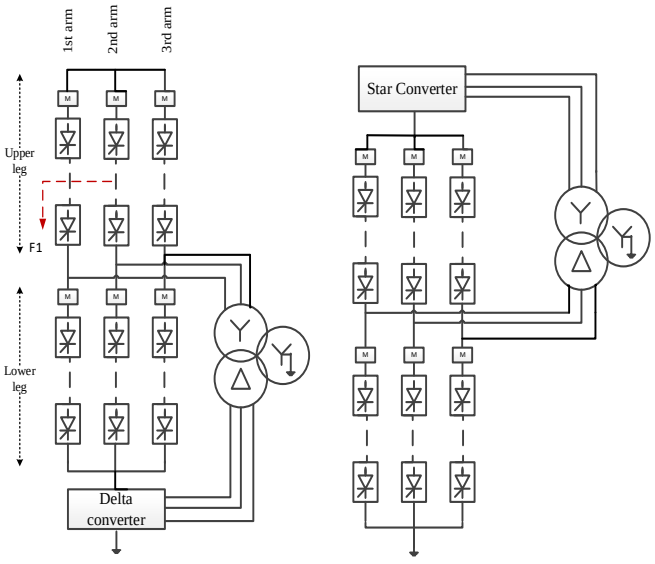

Fig. 2. Internal structure of the twelve-pulse converter.

In this study, the diagnostic algorithm uses the individual arm currents measured at the upper terminals of the thyristor arms, denoted by the "M" points in Fig. 2. These measurement points are located on the DC-fed side of each arm, between the smoothing reactor / DC bus and the corresponding thyristor stack. Therefore, the currents are acquired directly in the DC arm branches. In practice, non-intrusive Hall-effect or optical current transducers can be installed on each monitored arm. Because the proposed method relies on the cycle-averaged (DC) component of these currents, a modest sensor bandwidth of about 2–5 kHz is sufficient, and no high-frequency transient information is required.

III. The Control System

Fig. 3 depicts the equivalent circuit of the studied HVDC system, where the DC network is represented by a fundamental inductance L and a series resistance R. The values of L and R represent the inductance and resistance of the smoothing inductor and DC line, respectively. The voltages V_{dr} (rectifier voltage across the terminals) and V_{di} (inverter voltage across the terminals) are defined according to (1) and (2).

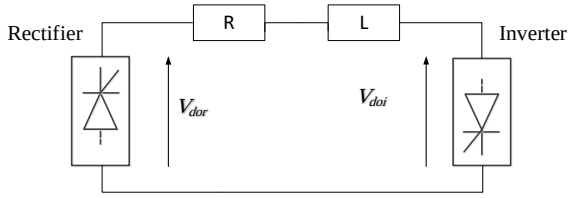

Fig. 3. Equivalent circuit of HVDC system.

$$V_{dr} = V_{dor}\cos\alpha - R_{cr} I_d \quad (1)$$

$$V_{di} = V_{doi}\cos\gamma - R_{ci} I_d \quad (2)$$

Where V_{dor} is the rectified voltage dependent on the AC voltage of the rectifier side, and V_{doi} is the inverter voltage dependent on the AC voltage of the inverter side. I_d is the DC line current, and α is the firing angle. If μ is the commutation angle, the extinction angle is defined as $\gamma=\pi-\alpha-\mu$.

According to the equivalent circuit and considering (1) and (2), the DC current can be written as (3) and (4).

$$I_d = (V_{dr} - V_{di})/R \quad (3)$$

$$I_d = (V_{dor}\cos\alpha - V_{doi}\cos\gamma)/(R + R_{cr} - R_{ci}) \quad (4)$$

According to (3), the DC current magnitude is directly proportional to the voltage differential measured between the rectifier and inverter terminals. Furthermore, the control factors I_d include the firing angle α, the extinction angle γ, and the AC voltages of the rectifier and inverter sides.

In most HVDC systems operating optimally, the rectifier controls DC current while the inverter regulates the DC voltage. Fig. 4 illustrates the corresponding V-I control characteristic and identifies the system operating point (Q) in this mode. According to (4), and considering that the firing angle α is maintained in the range of 2 to 5 degrees to ensure sufficient thyristor turn-on voltage. The constant alpha characteristic is plotted in the diagram of Fig. 4.

The constant alpha characteristic (line AB in Fig. 4) applies when the AC voltage on the rectifier side suddenly decreases, and according to (1), the system compensates for this by decreasing α. As a result, the system enters the constant alpha state and maintains a constant value of α at 2 degrees. According to the diagram in Fig. 5-a, in this case, the rectifier and inverter diagrams may not have an intersection point. As a result, the inverter enters the constant current state, and the operating point is located at (S). Since the value of the inverter current is usually less than the rectifier current, the marginal value of the current is considered to be 0.1, as indicated by ΔI_d in Fig. 4.

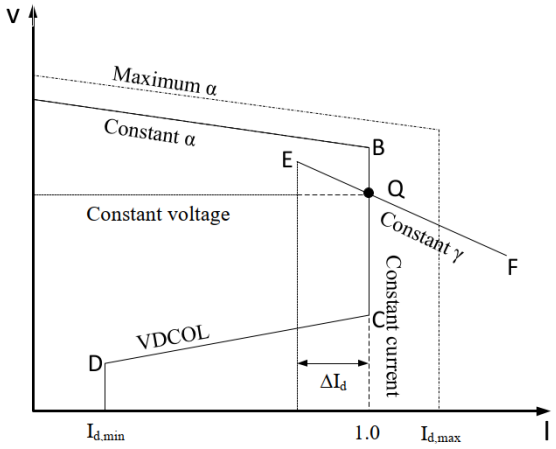

Fig. 4. Current-voltage characteristic of DC system.

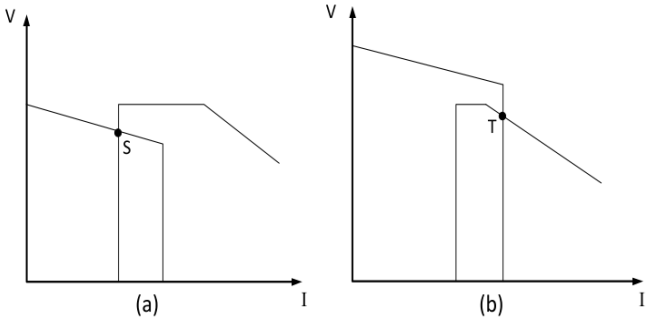

Fig. 5. Current-voltage characteristic of DC system during AC voltage drop on the a) rectifier side, b) inverter side.

On the other hand, by reducing the AC voltage on the inverter side, to prevent the occurrence of commutation failure, the inverter enters the constant gamma mode (line EF in Fig. 4). It keeps the value of γ constant at its minimum allowable value. The operating point of the system in this mode is indicated by (T) in Fig. 5-b [18], [19].

To protect thyristors from overheating at high currents, the maximum DC current ($I_{d,max}$) must be kept below 1.2 per unit. Similarly, to maintain continuous current flow and prevent dangerous chopping, the minimum current ($I_{d,min}$) must stay above 0.2 per unit. These operating limits are shown in Fig. 4.

The voltage-dependent current order limiting (VDCOL) characteristic, represented by line CD in Fig. 4, proportionally reduces the reference current during DC voltage depressions caused by DC faults or severe AC faults. This reduction subsequently decreases AC system reactive power consumption, facilitating faster grid recovery during fault conditions.

In the inverter, the values of α_{min} and α_{max} are defined to ensure that the inverter does not enter the rectifier mode and to create the necessary margin for the minimum extinction angle, respectively. Moreover, following DC faults, the absence of current zero crossing prevents arc extinction. Consequently, fault-induced arcs persist even after fault clearance. To deal with this situation, after 0.07 seconds a forced alpha mode is activated in which the rectifier enters the forced alpha mode and its alpha value is kept constant at 166 degrees, as a result of which the rectifier operates in the inverting mode and the system energy is discharged from the two rectifier and inverter terminals and the electric arc caused by the fault is extinguished [18].

IV. Proposed Method

Faults within the converter can be caused by factors such as thyristor arm malfunction, failure of associated components, inverter commutation failure, or an internal converter short circuit. This paper aims to investigate the short-circuit fault in thyristor arms within the inverter.

In reference [20], a short circuit fault in the thyristor arms of the rectifier is investigated. Since this fault current contains a DC component and exhibits no zero crossing, the resulting electric arc persists after fault clearance. Due to the rectifier's AC network supply, this internal converter fault effectively manifests as a permanent short circuit fault on the AC network side. Consequently, by measuring the transformers' secondary current and detecting both the DC component magnitude and direction, the fault location (specific arm or phase) can be identified. This enables fault elimination through selective single-phase switching on the transformer primary winding. However, this mitigation strategy is ineffective for inverter-side faults. Because the inverter is DC fed, single-phase switching on the inverter side transformer is operationally ineffective.

Although the forced alpha method can discharge system energy and restore operation during transient faults, locating the fault becomes critical for inspection and maintenance when encountering permanent faults, repeated faults, or control system malfunctions.

Since the fault is DC network fed, during a leg fault, the current in the lower thyristor legs collapses to zero, and the DC current component diverts exclusively through the upper bus to the faulted leg. According to Fig. 2, an SL1 fault causes current collapse in all delta-connected (D) arms while the DC current component persists exclusively within the star-converter legs. Furthermore, because the delta converter's lower phase leg is grounded, a short circuit fault here only reduces current magnitude without typical short circuit effects.

V. Simulation Results

This paper proposes a fault detection method based on measuring arm currents within the converters and analyzing their DC components. The approach enables precise fault location identification, allowing targeted inspection or preventive measures to be implemented on the affected converter arm.

The network analyzed in this study is derived from Hydro-Quebec monopolar HVDC system. This system demonstrates robust fault management capabilities, effectively detecting both DC and AC faults while maintaining optimal control during fault conditions. However, the system cannot detect internal converter faults.

This section simulates multiple short-time faults (0.7–0.78 s) across different inverter arms and discusses the results. First, system behavior is evaluated without forced alpha operation.

Figs. 6 and 7 depict SU2 and SL2 currents on the inverter side during a short circuit fault in SU2.

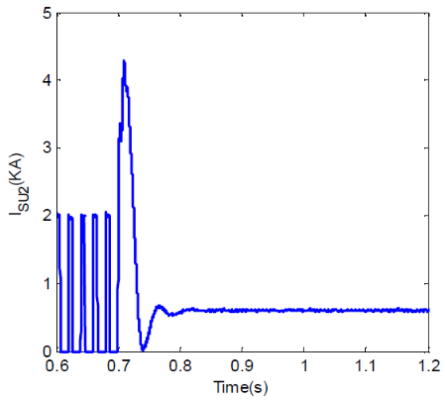

Fig. 6. SU2 current during short circuit fault in SU2.

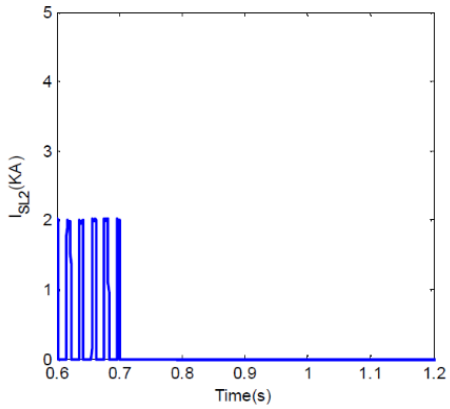

Fig. 7. SL2 current during short circuit fault in SU2.

Figs. 8 and 9 also depict the change in the converter control mode and the inverter reference current when this fault occurs. The control modes include 0 for block mode, 1 for constant current, 2 for constant voltage, 3 for minimum alpha, 4 for maximum alpha, 5 for forced alpha, and 6 for gamma control.

Since the fault is fed from the DC line side, when a short circuit fault occurs in SU, the current in SL, DU, and DL becomes zero. During DC faults, the control system reduces the reference current according to the VDCOL characteristic in response to a reduction in DC voltage. This action forces the inverter into current control mode, thereby reducing the magnitude of fault current. Due to the DC current component and the absence of zero crossing, the fault-induced electric arc persists. After fault clearance, this current continues to circulate within the faulted section. As the inverter voltage drops to zero, it loses control of the system voltage and current, and the inverter enters the maximum alpha state.

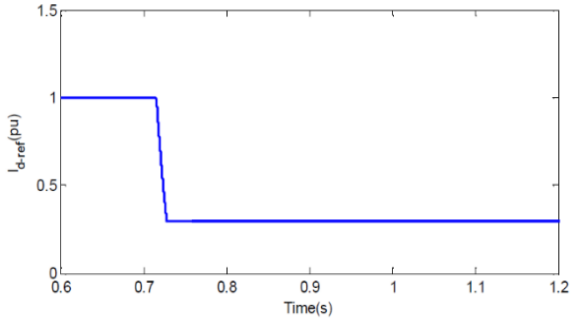

Fig. 8. Control modes changes in the inverter during a short-circuit fault in SU2.

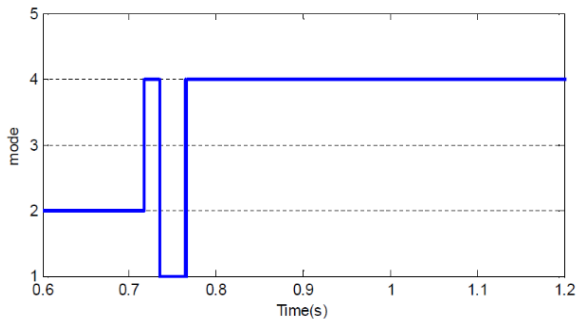

Fig. 9. Reference current changes in the inverter during a short-circuit fault in SU2

Figs. 10 to 12 depict SU1, SL1, and DU1 currents on the inverter side during an SL1 short circuit fault. Figs. 13 and 14 show the corresponding converter control mode variations and inverter reference current dynamics under this fault condition. As with prior fault, DC voltage reduction during this fault activates the VDCOL function. The resultant reference current decreases the DC current, causing the inverter to enter current control mode.

However, in this scenario, the current reduction extinguishes both the electric arc and the fault current. Consequently, the inverter maintains current control mode, restoring the network to its pre-fault state by ramping up the reference current. As illustrated in Fig. 2, the fault current path flows through SU. During such faults, SU manifests overcurrent while DC current appears in both star converter legs; meanwhile, delta-converter currents collapse completely to zero.

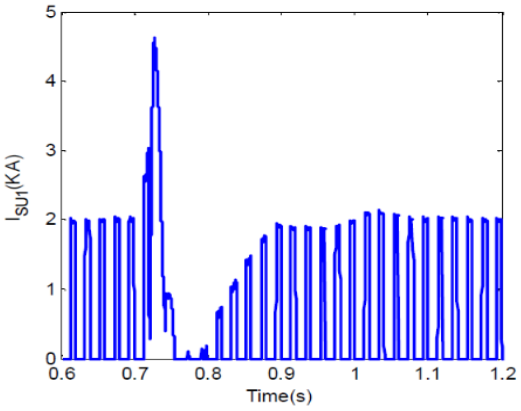

Fig. 10. SU1 current during short circuit fault in SL1.

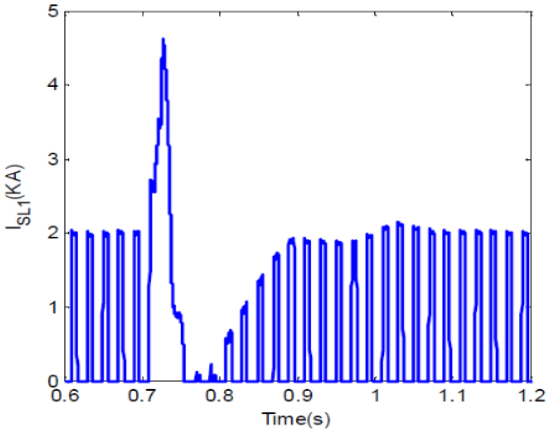

Fig. 11. SL1 current during short circuit fault in SL1.

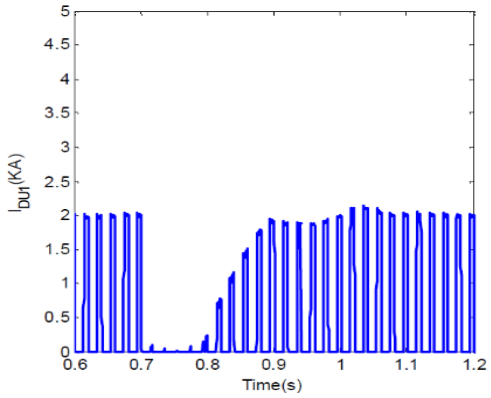

Fig. 12. DU1 current during short circuit fault in SL1.

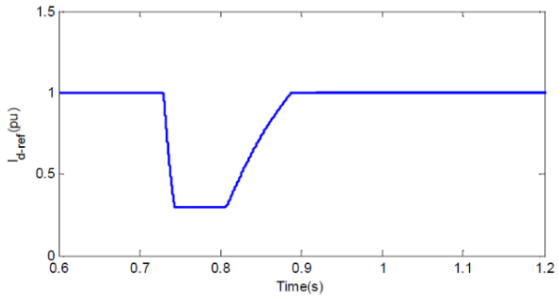

Fig. 13. Control modes changes in the inverter during a short-circuit fault in SL1.

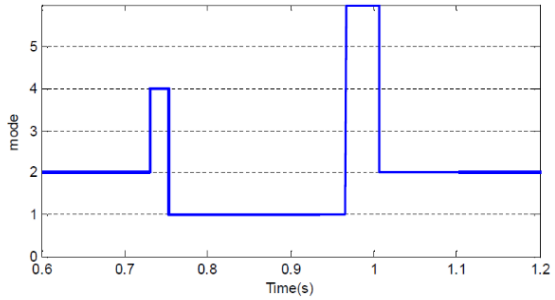

Fig. 14. Reference current changes in the inverter during a short-circuit fault in SL1.

Figs. 15 to 17 depict SU1, SL1, and DU2 currents on the inverter side during a DU2 short circuit fault. Figs. 18 and 19 show converter control mode variations and inverter reference current dynamics under this condition. As fault current rises and DC voltage drops—consistent with prior cases—VDCOL reduces the reference current, triggering the converter's transition to current control mode. Fig. 2 confirms that at fault initiation, both star converter legs and the faulted arm simultaneously manifest overcurrent accompanied by DC component generation. However, similar to SL fault cases, the star converter's fault current ceases completely, allowing uninterrupted continuation of normal operation.

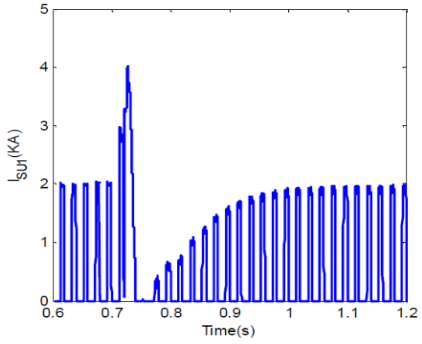

Fig. 15. SU1 current during short circuit fault in DU2.

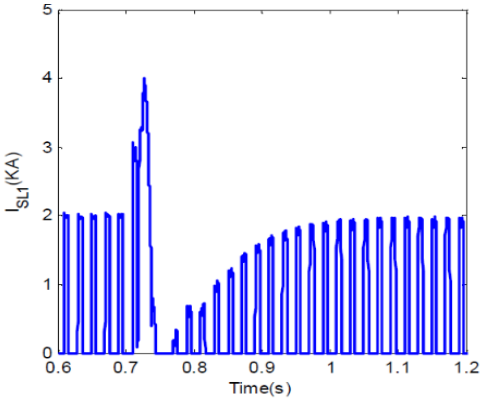

Fig. 16. SL1 current during short circuit fault in DU2

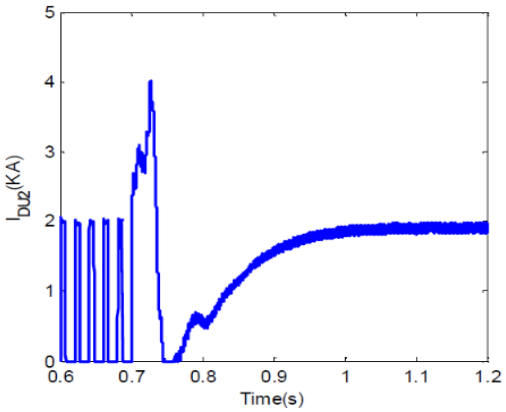

Fig. 17. DU2 current during short circuit fault in DU2.

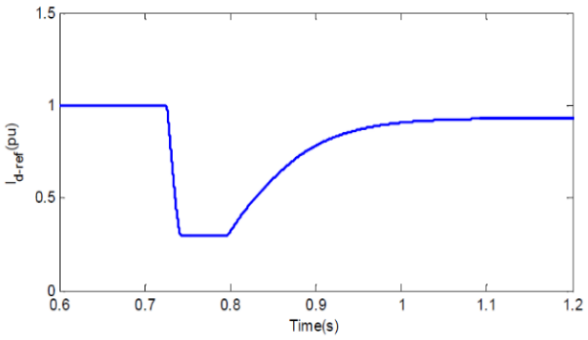

Fig. 18. Control modes changes in the inverter during a short-circuit fault in DU2.

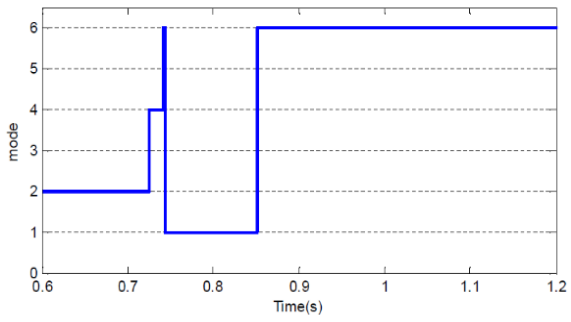

Fig. 19. Reference current changes in the inverter during a short-circuit fault in DU2.

In fact, the inverter maintains current control mode, increasing the reference current to 1.0 pu after the star converter fault clearance. However, the electric arc persists in the delta converter, sustaining localized current circulation at the fault point. Consequently, the inverter's operation resembles a 6-pulse converter. Due to the primary current path configuration, current cannot reach the delta converter's lower phase leg. Until fault extinction, this leg's current

persists at zero, prompting the system to engage gamma control mode to prevent commutation failure.

Since the delta converter's lower phase leg is grounded, short-circuit faults in this leg become electrically insignificant and need not be investigated.

Simulations in this section omitted forced alpha mode operation. Consequently, the presence of DC components in arm currents and current collapse in non-faulted arms enables unambiguous identification of the faulty leg and arm.

When forced alpha operation is active:

- For SU/DU faults: VDCOL reduces the reference current to lower the fault current, triggering forced alpha activation. Increasing α to 166° discharges system energy bidirectionally, extinguishing the transient fault arc.
- For SL faults: The fault arc self-extinguishes without requiring forced alpha intervention.

However, for permanent faults, recurring faults, or control system failures, a fault location algorithm becomes essential. This enables targeted inspection, repair, or preventive measures.

Figs. 20 to 22 present simulation results for short circuit faults across various converter legs under forced alpha operation.

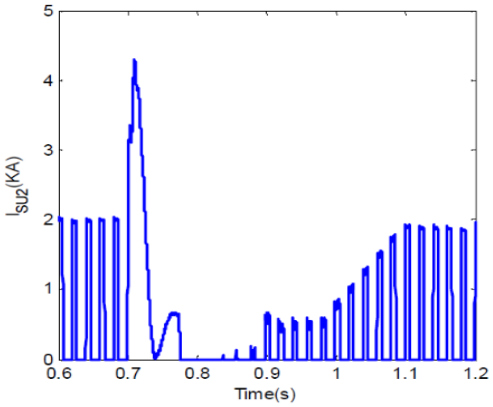

Fig. 20. SU2 current during short circuit fault in SU2 with forced alpha mode activated.

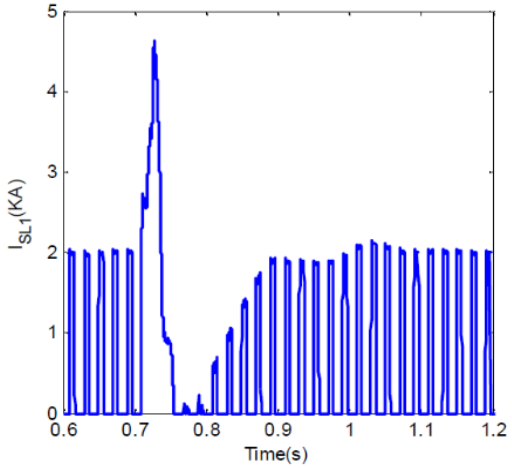

Fig. 21. SL1 current during short circuit fault in SL1 with forced alpha mode activated.

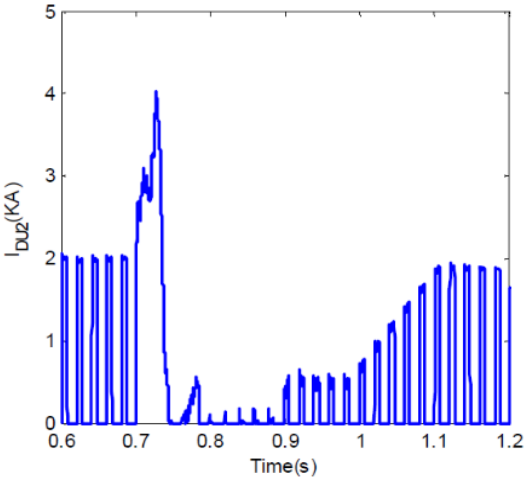

Fig. 22. DU2 current during short circuit fault in DU2 with forced alpha mode activated.

As demonstrated in the figures, forced alpha activation extinguishes the fault. Crucially, identification of the faulty arm must precede this activation. In all cases, one or two upper leg arms exhibit DC component currents, with current collapse occurring in the lower legs of the affected converter section. Given that forced alpha mode activates 70 ms post-fault inception, a dedicated algorithm must detect and locate faults before forced alpha initiation.

VI. Protection Method Algorithm

During normal operation, each converter arm conducts current for 60 electrical degrees (one-third of a cycle) and remains at zero current for 120 electrical degrees (two-thirds of a cycle). However, during an arm short circuit fault, lower leg arm currents collapse to zero while the faulted arm conducts continuously for multiple cycles. This distinct behavior forms the foundation of the fault detection algorithm.

A fault in a given arm is confirmed if its current remains non-zero for 40 ms (two cycles) while all lower leg arms maintain zero current throughout this interval. Figs. 23 and 24 show the proposed algorithm. According to Figs. 23 and 24, Algorithm A initially executes across all four inverter-side converter legs, numbered 1 to 4 sequentially from top to bottom. In the Algorithm of Fig. 23, the arm current integral (C_j) and DC line current integral (d) are measured over one cycle. If these two parameters are equal, the arm is short-circuited to the DC line current. To ensure valid fault determination, the Algorithm of Fig. 23 requires that the value of $|C_j\text{-}d|$ be less than a threshold value (Δ_{th}) for two consecutive cycles.

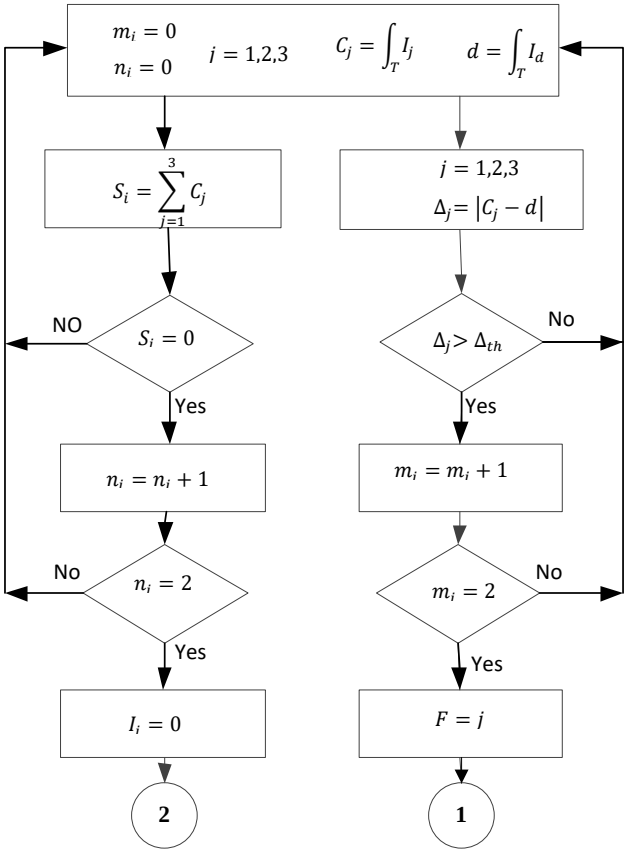

Fig. 23. Algorithm for measuring the average current in the inverter arms (algorithm A)

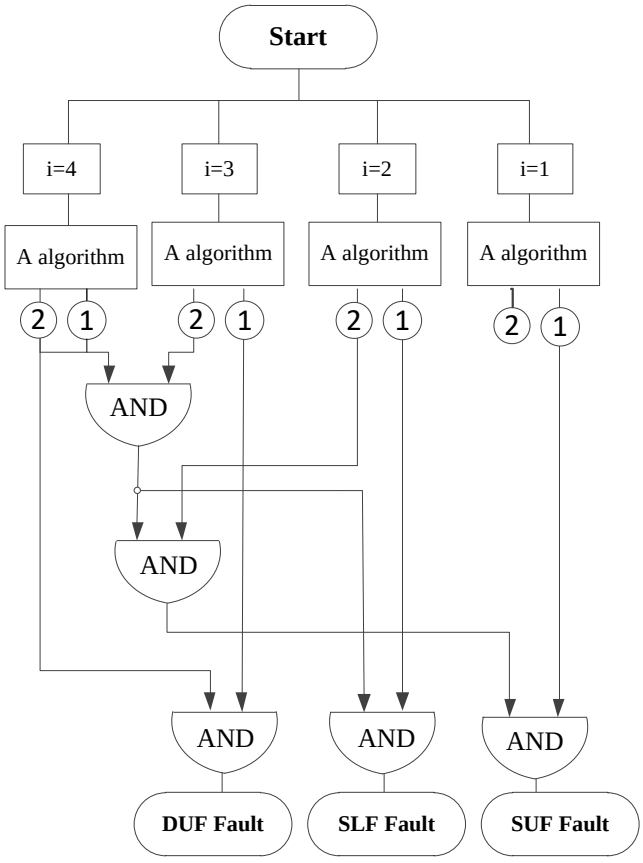

Fig. 24. Proposed fault detection for inverter arms

Since the fault feed path originates from the DC line, the current in the upper legs that are short-circuited can also apply to this condition. Therefore, the condition of zero current in the lower legs must also be checked.

In Algorithm of Fig. 23, the sum of the integral currents of all three arms in one leg (S_i) is also calculated, and if this value is zero during two cycles, it means that no current is entered this leg, which could be due to a short circuit in the upper legs. Finally, in the algorithm of Fig. 23:

- Output 1 activates if any arm current equals the DC line current for 40 ms.
- Output 2 activates if the leg current sum *Si*=0 persists for two consecutive cycles.

In the Fig. 24 algorithm, Outputs 1 and 2 from Fig. 23 serve as inputs. When active, they trigger validation of two concurrent conditions:

- Arm current continuity ($|Cj-d|<\Delta th$)
- Zero current in all lower arms

Both conditions must persist for 40 ms to confirm fault localization. When an arm's current equals the DC line current concurrent with zero current in all lower legs, this confirms a short-circuit fault in that specific arm. The faulted arm and its parent leg are thereby definitively localized.

Since the proposed method detects the fault through the cycle-averaged (DC) component of the arm currents, it is inherently less sensitive to sensor inaccuracies than high-frequency or transient-based protection schemes. Sensor offset has a negligible impact on the decision logic because the fault indication is obtained by comparing the integral of the arm current with the integral of the DC line current, causing constant offsets to cancel each other out. Long-term drift may shift the threshold Δth slightly, but the fault signature (persistent arm current with simultaneous current collapse in the lower legs) remains unaffected; drift can be mitigated through periodic calibration. Bandwidth requirements are modest, as only the fundamental-frequency waveform needs to be captured; a bandwidth of 2–5 kHz is adequate. Sensor saturation is unlikely because the arm currents remain within the continuous-measurement range of standard Hall-effect or optical transducers commonly used in HVDC converters.

For practical implementation, the algorithm requires only cycle-averaged arm-current values. Therefore, a sampling rate of 20–40 samples per electrical cycle is sufficient, corresponding to approximately 1–2 kHz for 50/60 Hz power systems. No high-frequency transient components are needed, and the method remains fully effective at these modest sampling rates.

The proposed algorithm has a very low computational burden, as it requires only cycle-by-cycle integration of arm currents and simple comparison operations. No frequency-domain processing or high-rate sampling is needed. Therefore, the method can be executed on typical DSP- or FPGA-based HVDC control platforms with negligible CPU load and memory usage (only two cycles of data are stored). The latency of the implementation is well below the two-cycle detection window, making the algorithm suitable for real-time industrial deployment.

In practical HVDC installations, arm-current measurements are affected by EMI and sensor noise. However, the proposed algorithm relies on the cycle-averaged (DC) value of the arm currents, which inherently suppresses high-frequency disturbances and makes the method robust to typical measurement noise. Only severe sensor drift or loss of

measurement may affect detection, while moderate noise does not alter the integral-based decision criteria. If required, a simple moving-average or low-pass filter may be applied to the measured currents; such filtering does not impact the detection time because the algorithm already operates over a 20–40 ms evaluation window. From a computational perspective, the algorithm consists mainly of three numerical integrations and threshold comparisons, resulting in a negligible computational burden. Consequently, it can be executed on standard DSP-based HVDC controllers or small FPGA devices with minimal latency and very low memory usage (only one or two cycles of samples are needed). Thus, the method is fully compatible with practical HVDC protection hardware.

VII. Limitations and Discussion

The proposed detection mechanism is based solely on the DC-fed nature of current-source converter arms and the characteristic collapse of the lower-leg currents during internal arm faults. Therefore, the same principle applies to bipolar HVDC links, where the two poles can be evaluated independently. In multi-terminal CSC-HVDC systems, the arm-level detection principle remains valid; however, coordination with station-level protection may be required due to the more complex current-sharing behavior. The method assumes a conventional thyristor-based CSC structure, and substantially modified converter topologies may require adjustments of the detection thresholds.

The applicability of the proposed method is governed by the characteristic current signatures produced by internal arm faults. Internal faults create a persistent DC component in the faulted upper arm and cause all lower-leg currents in the same converter section to collapse. In contrast, severe DC-line faults depress all arm currents simultaneously without generating a localized DC offset. This inherent difference enables reliable discrimination between the two fault categories. The algorithm is also capable of handling evolving or sequential faults, as the decision logic is based on the cycle-by-cycle evaluation of the arm-current integrals. Simultaneous multi-arm faults can be detected, but may require coordination with station-level protection if their signatures become ambiguous. The method is most effective for low- and medium-impedance internal faults; very high-impedance faults may produce a weak DC component, in which case auxiliary protection functions may be needed.

VIII. Conclusion

This study presents a novel and efficient approach for precise short-circuit fault localization in inverter arms of CSC-HVDC systems. By relying solely on arm current measurements, the proposed method eliminates the need for voltage sensors while maintaining high diagnostic accuracy. The algorithm, based on current integration, deterministically identifies the faulty arm within two electrical cycles (about 40 ms) and operates effectively without high-rate sampling or computationally intensive processing. The method was rigorously validated through comprehensive simulations under both forced-α operation and normal operating conditions. Results demonstrate that it consistently achieves fault localization within 40 ms—fast enough to enable preventive isolation before significant energy discharge occurs. For permanent faults, the capability to pinpoint the exact faulty arm enables targeted maintenance, allowing for the rapid isolation and replacement of damaged components and thereby minimizing system downtime.

In the proposed method, the fault detection time is on the order of two network cycles. Due to its reliance on the DC component of the arm current, a high sampling rate is not required; sampling rates of a few kilohertz are sufficient for effective signal extraction. In contrast, wavelet-based methods typically require much higher sampling rates (tens to hundreds of kHz) and longer processing times due to the multi-stage nature of wavelet analysis. AI-based approaches, especially those using neural networks or deep learning algorithms, have detection times dependent on the model size and complexity, often resulting in higher computational delays and the need for more powerful hardware.

Regarding computational load, the proposed method only requires the calculation of the instantaneous current integral and comparison of DC values. Therefore, it is significantly lighter than wavelet methods, which involve multi-level signal decomposition, and AI-based methods, which require feature extraction, model training, or execution of complex networks. This makes it feasible for implementation on standard HVDC controllers with limited computational resources.

In terms of accuracy, although wavelet and AI methods may achieve high performance under laboratory conditions, their strong dependence on signal quality, parameter tuning, and high sampling rates can reduce their effectiveness in noisy industrial HVDC environments. In contrast, the proposed method, due to the DC nature of the detection index and the high current levels in CSC-HVDC, is less sensitive to noise and has demonstrated stable and fast detection of internal arm faults under simulated conditions.

Therefore, based on this qualitative comparison, the main advantages of the proposed method over wavelet- and AI-based techniques are its simplicity, low sampling rate requirement, minimal computational load, and short detection time. However, precise numerical comparisons can be addressed in future studies.

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Conflicts of Interest

The author declares that there is no conflict of interest regarding the publication of this article.

Authors' Contributions

Conceptualization and study design: (F.F.M. & A.M.)
Data collection and experimentation: (F.F.M.)
Data analysis and interpretation: (All)
Manuscript writing and editing: (All)
Supervision and project administration: (A.M.)

STATEMENT ON THE USE OF GENERATIVE AI

AI cannot be listed as an author. Only human authors take responsibility.

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