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# Design of a Ddsm Modulator to Reduce Hardware and Power Dissipation in Fractional Frequency Synthesizers

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***Abstract*—The output of a Digital Delta-Sigma Modulator (DDSM) is always a periodic signal, and the input is constant. A hybrid DDSM is a premiere to its conventional counterpart for having a potential speed, by the choice of its smaller bus. Random techniques and deterministic methods are two strategies to maximize the periodicity. The dither signal is used in the random approach to enhance the signal cycle. The deterministic procedure causes the modulator's internal structure to alter. The majority of randomized approaches eliminate spurious tones. A novel approach for the DDSM modulator is suggested in this paper to improve the output period while reducing the undesired tones. Modulators with different word lengths are proposed in this paper. The length of the input word is divided into several parts, and each part is entered into a modulator to reduce hardware consumption. Consequently, the power consumption is decreased. Moreover, in this structure, the dither signal is used to change the alternating state of the output and reduce the spurious tones. Also, a four-stage modulator is proposed, each part of which has special characteristics. In this paper, a hybrid digital sigma-delta modulator is proposed that has lower power consumption than previous methods and reduces the number of transistors. In addition, there are fewer spurious tones in the output power spectrum of this modulator. The simulation results with 0.18 µm CMOS technology by HSPICE application show that 2530 transistors are used, which is a 15% decrease compared to the conventional method.**

***Index Terms*- Digital Sigma Delta Modulator, Hardware Reduction, Power Consumption, Separate Lines, Spurious tones.**

## I. Introduction

With the advancement of digital technology, the importance of analog-to-digital converters (ADC) has increased. Among various types of ADCs, the delta-sigma modulation ADC is frequently used for high-resolution applications. This is because the ability of the delta-sigma ADC to produce high resolution without the need for high-accuracy analog components is a significant advantage [1-3]. The delta-sigma ADC is composed of a digital filter and a delta-sigma modulator (DSM). A one-bit pulse density modulated digital sequence (PDM) is produced from an analog signal by the DSM at a frequency that is much greater than the Nyquist rate. After that, the PDM is converted into a multi-bit digital signal via the Nyquist rate filter.

The DSM is the primary factor governing the ADC's accuracy and resolution. A one-bit sampler, an integrator, and a feedback digital-analog converter (DAC) make up a standard DSM. In this case, the integrator and feedback DAC limit how quickly the DSM may operate. A Voltage Controlled Oscillator (VCO) is used in the Frequency Delta-Sigma Modulator (FDSM), a different kind of DSM that has garnered a lot of interest lately [4–15]. Without a feedback DAC or integrator, the FDSM operates on an FM signal (intermediate frequency modulation) produced by the VCO. It is therefore appropriate for high-frequency operation. Thus, the modulator type in question contains fewer components. This paper's primary goal is to reduce VCO phase noise to

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reduce sigma-delta modulation noise. The other elements of sigma-delta modulation are designed to reduce the number of transistors. To achieve this, the gate diffusion technique is used to design XOR and some other vital elements. Electro-optic modulators are an indispensable part of photonic communication systems, largely dictating the achievable transmission rate. Recent advances in materials and fabrication/processing techniques have brought new elements and a renewed dynamic to research on optical modulation. In [18, 19], a novel structure for an all-optical amplitude modulator (AOAM), with a high extinction ratio (ER), is proposed. A nano-disk resonator (NDR), a ring-shaped resonator (RR), and perpendicular waveguides (WGs) are used for the realization of the proposed topology. Due to the symmetrical structure of the designed AOAM, each of the two WGs can be considered as the data WG and the second one can be selected as the control WG. Since there is a suitable isolation between data and control signals in this method, the proposed structure is much more suited for integrated optics compared to the aforementioned modulators which are published in the literature. Also, to separate the control wavelength from the data wavelength, a graded stub filter is designed and located at the output port of the AOAM.

The structure of this document is as follows. The FDSM's working concept and the gate diffusion technique's element design are explained in Section 2. The suggested method for phase noise reduction of the delta-sigma VCO is presented in Section 3. This study is finally summarized in Section 4.

## II. Methodology

Vector samplers and Nyquist rate converters are the two broad categories into which analog-to-digital and digital-to-analog converters fall. Nyquist exchangers are very accurate and fast. Vector converters, on the other hand, are quite accurate in low-speed applications. These converters modify the sampling rate for high-precision access, which are relatively cheaper than Nyquist converters. An example of such a modulator is the sample Sigma Delta ADC converter. A sample Sigma Delta ADC converter includes a linear time-independent grid with two inputs, one output, and a one-bit Q quantizer. This quantizer is located in the feedback network. Sigma Delta modulation increases the effective accuracy of the quantizer by sampling and noise formation. Modulators can be implemented using either a data sampling method or a continuous method. Continuous time systems employ active RC integrators, whereas sampling systems utilize capacitive switch integrators. Depending on the amplitude axes and the time of the input signal, the modulators are divided into three categories.

1 - Continuous time (CT)
2 - Discrete time (DT)
3 - Digital Delta Sigma Modulator (DDSM)

The DDSM Modulator is the preeminent manufacturer of synthesizers operating at fractional frequencies. A block diagram of a phase-lock loop (PLL) synthesizer featuring a module regulated by the DDSM modulator is depicted in Fig. 1.

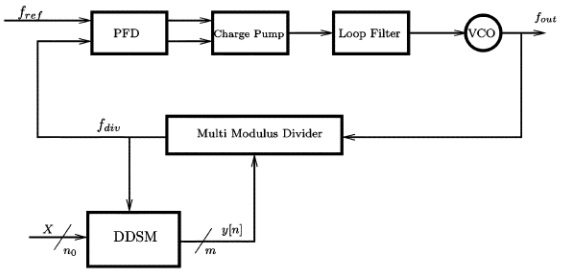



Fig. 1. Frequency synthesizer block diagram controlled by Sigma Delta modulator

The circuit includes a phase-frequency detector (PFD), a load pump circuit, a loop filter, a voltage-controlled direct oscillator, and a multi-module divider controlled by a DDSM modulator in the feedback path. The DDSM modulator regulates the split ratio of the divider, and the required decimal ratio is equal to the average split ratio at the number of periods above the reference frequency. The input of DDSM is a high-precision digital $X$ signal that adjusts the decimal division ratio, and the output of the low-precision string modulator $y[n]$, which controls the value of the divider.

Inputs and outputs of the DDSM Modulator are both digital. The modulator is designed to accept an input string $X$ of length $n_0$ and generate an output string $y$ of length $m$. In addition to the principal input range, the DDSM modulator generates a low-precision string at its output. In the output signal spectrum, there is accurate input information. Ideally, quantization noise is white, and its power is transmitted outside the signal band, which is called noise formation. If the output signal is applied to an ideal continuous-time low-pass filter that passes only low-frequency output, then the main input signal will be extracted from the low-precision output signal with a high signal-to-noise ratio. The output signal power is much higher than the noise power.

A significant application of DDSM modulators is the conversion of data from digital to decimal and analog frequency synthesizers. The phase lock ring is another essential component of wireless transmitter/receiver systems. Typically, these synthesizers produce objectionable phase noise. Considering the utilization of DDSM in wireless transmitters and receivers, we attempt to analyze several critical attributes of these devices. One of these important features in DDSM modulators is the presence of noise in terms of intermittent modulation signals with a fixed input. The structure of the modulator, the initial conditions, the input, and the modulus of the quantizer all influence the period of quantization noise. The hardware consumption and power level of DDSM modulators, including the requisite number of transistors and gates, are also crucial characteristics. Other structures examined include Multistage noise Shaping structures (MASH), Single Quantizer (SQ), and feedback error modulator (EFM).

The DDSM Modulator is a finite-state machine (FSM) with a finite number of states that is constructed utilizing several precise computational units. Every FSM has a different rule for transitioning between states. Every state follows the one before it instantly if the input is fixed. The shorter the output cycle, the greater the power of the spurious tones. The presence of these tones in the output power spectrum greatly reduces the SFDR range of the modulator. Therefore, the output period should be maximized. There are two methods to increase periodicity, which are: random methods and deterministic methods. The random approach lengthens the

output period by means of a dither signal. The modulator's internal structure is altered using the definitive approach. Most randomized methods reduce spurious tones and increase the period of quantization noise. In the random method, a single-bit quasi-random signal called dither is usually used to change the alternating state of the output string. The disadvantage of random methods is that they create noise in the output spectrum, and hardware consumption increases in terms of using a dither signal generator circuit. This paper provides a way to design DDSM modulators. This method is based on separate lines, which is applied to DDSM modulators with and without dither, and fixed inputs. Modulators' word lengths are optimally selected to reduce hardware and power consumption. Therefore, the digital input will be divided into several parts, and several modulators with appropriate word lengths will be used.

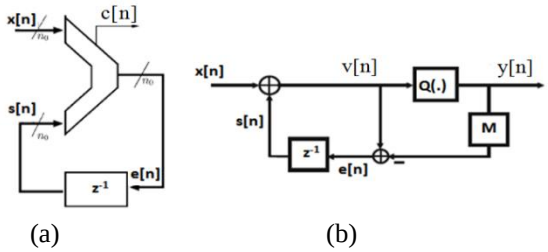
## III. The Proposed Method

From a digital storage, the initial block diagram of a multi-stage MASH modulator is generated. The model of the accumulator is illustrated in Fig. 2. When expressed in this manner, the input to the storage consists of the n-bit digital word *x[n]*. The input to fractional frequency synthesizers remains constant while the user configures the intended fraction value of $\frac{X}{2^{n_0}}$. By one unit of time, the string stability of the error *e[n]* is delayed. The sum of the delay string *s[n]* and the input signal *x[n]* is calculated. When the accumulator overflows, bit *c[n]* of the transport sequence is set to one. The number of ones and zeros comprising the average time of the output string is identical to the average time of the input. Fig. 2-b illustrates the model of digital storage. The quantizer *Q(.)* and the output digit *c[n]* are represented by the output string *y[n]*. This pertains to the operation of warehousing excess. Overflow occurs when the signal *v[n]*, which is equal to the sum of the signals *x[n]*, *s[n]*, exceeds or equals $M = 2^{n_0}$. In such a case, *y[n]* = 1. If not, the value is zero. Numerically, we therefore have [11]:

$$c[n] = y[n] = Q(v[n]) = \begin{cases} 0, & v[n] < M \\ 1, & v[n] \geq M \end{cases} \quad (1)$$

The register is used to feed the difference between v [n] and *My[n]* to the input; if *y[n]* = 0, then *e[n]* = *v[n]*, and if *y[n]* = 1, then *e[n]* = *v[n]* -*M*. Thus, we have [11]:

$$e[n] = v[n] \mod M \quad (2)$$




(a) (b)

Fig. 2. a) The digital accumulator used in the MASH structure b) Its model

This structure is referred to as EFM, as the error signal *s[n]* is looped back to the storage input. Fig. 3 depicts the block design of a first-order DDSM modulator. It is composed of a series connection of $EFM_1$ n-bit blocks and a noise cancellation network. This negative structure eliminates the quantization error of the intermediate stages by passing the quantization error of each stage to the subsequent stage and the output of each stage into the noise cancellation network. The consequent equation represents the *z*-domain output of the MASH modulator of the first order [12].

$$Y(z) = \frac{1}{2^N}.X(z) + \frac{1}{2^N}(1 - z^{-1})^l.E_l(z) \quad (3)$$

The name for each DDSM modulator is $DDSM_l$. Our objective is to investigate a critical component of DDSM modulators. The hardware and power consumption of a DDSM modulator are detailed below. Typically, the power spectrum is free from undesired tones. In practice, the power spectrum of most DDSM modulators contains spurious tones. The shorter the output cycle, the greater the power of spurious tones. The presence of these units in the output power spectrum greatly reduces the SFDR range of the modulator. In the decimal synthesizers, the presence of spurious tones in the spectrum is extremely problematic, creating nonlinear effects in the implementation of pump circuits, frequency detectors, filters, and VCO circuits, and transmitting carrier out-of-phase phase noise to the inbound. Therefore, it is necessary that the quantization noise is white and independent of the modulator input. A strong correlation between the circuit input and quantization noise can cause spurious tones in the output spectrum. To send their power outside the signal band, the DDSM modulator shortens the simulated digital signal's word length and modifies the quantization noise that results. A short string quantization error string will cause spurious high-power tones in the modulator output range. This is a problem in applications, such as DAC converters and PLL circuits. Definitive and incidental techniques are used to investigate spurious tones in digital modulators. Definitive techniques maximize the length of the quantization error to minimize the power per ton. These methods are used in MASH digital modulators, SQ single-quantizer modulators, and EFM feedback error. Low-bit dither is used in DDSM modulators to eliminate spurious tones and uses two or more integrators in the quantizer lead path. The suggested approach reduces both the power consumption and hardware usage in terms of the quantity of logic gates and transistors used.

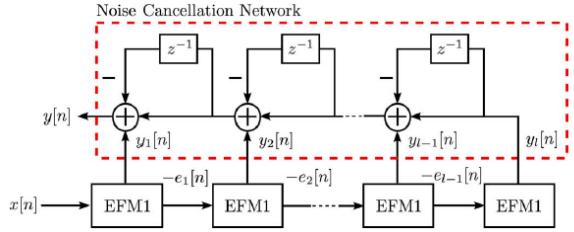



Fig. 3 Block diagram of first-order Sigma Delta MASH digital modulator [11]

This paper presents a new structure for MASH and EFM modulators, comprising different classes. Fig. 4 shows this new structure. In this figure, $M_i$ is the class *I* quantifier module.

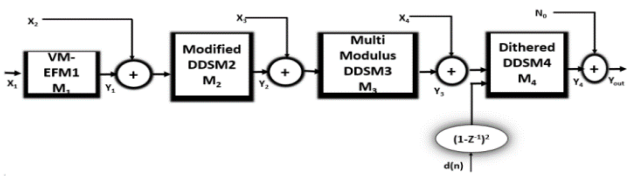



Fig. 4. Proposed method to reduce hardware and power consumption in DDSM modulators

In this structure, $X_1$ and $M_1$ should always be pseudo-prime numbers to try to maximize the output period of the

modulator. In this method, the input number is divided into several parts, and each part will be entered into a DDSM modulator. Besides, a filtered dither signal can be used at the circuit's input to reduce circuit noise and eliminate spurious tones. The first stage of this structure is a variable modulus EFM. This modulator is made of two adders, a multiplexer, and a NOT gate. The structure of this EFM modulator with a variable module is shown in Fig. 5.

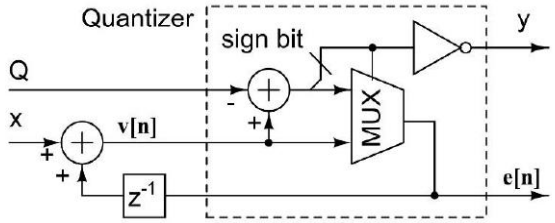



Fig. 5 Feedback error modulator structure with variable module

The second-order modulator is modified MASH 1-1, which has a conventional modulo $M_2$. A third-class multi-level modulator with several modules makes up the third stage. The signal amplitude to noise in this structure may be increased by using the feedback in the HK-MASH approach. The value of $a$, a tiny integer, is selected such that $2^{n_0}$ is smaller than the value of $M$-$a$ of the biggest prime number. With a second-order dither signal, the fourth stage is a fourth-class multistage modulator. A high-pass filter, the $V(z)$ filter, reduces the output spectrum's low-frequency region. This filter's conversion function is as follows [11].

$$v(z) = (1 - z^{-1})^2 \tag{4}$$

The fourth-order DDSM modulator is compatible with this filter. The fourth modulator in the hybrid proposed structure is dithered MASH 1-1-1-1, which is a periodic LFSR dither input with a period $N_d$ added to the third and fourth stages of MASH 1-1-1-1. This modulator has a high-pass filtered shaped dither signal. Fig.6 presents an implementation of the second-order dither hybrid modulator. To remove the quantization error of the middle classes from the previous part, the following step explains how to choose the right values for $N_{ISB}$, $N_{LSB}$, and $N_{MSB}$.

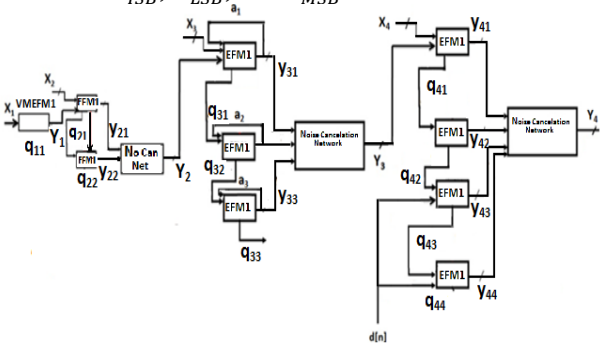



Fig.6: Implementation of the second-order dither hybrid DDSM 1-2-3-4 modulator.

The three-stage distinct line modulator's output may be represented as nested 1-2-3 in the following way [12].

$$Y_{123}(z) = \frac{X(z)}{2^N} + N_1(z) + N_2(z) + N_3(z) \tag{5}$$

Where

$$N_1(z) = \frac{1}{2^{N_{ISB}+N_{MSB}}.2^{N_{LSB}}}(1 - z^{-1}).E_1(z) \tag{6}$$

$$N_2(z) = \frac{1}{2^{N_{MSB}}.2^{N_{ISB}}}(1 - z^{-1})^2.E_2(z) \tag{7}$$

$$N_3(z) = \frac{1}{2^{N_{MSB}}}(1 - z^{-1})^3.E_{123}(z) \tag{8}$$

In the first-order modulator, $N_1$ represents quantized noise; in the second-order modulator, $N_2$ represents quantized noise; and in the third-order modulator, $N_3$ represents quantized noise. It is expected that the collected white sources are used to simulate all quantized sounds. As a result, $N_1$, $N_2$, and $N_3$'s power spectrum is (9) [17].

$$S_1(f[k]) = \frac{1}{12L_1}\left(\frac{1}{2^{N_{ISB}+N_{MSB}}}\right)^2 |1 - z^{-1}|^2_{z=e^{j2\pi k/L_1}}$$
$$S_2(f[k]) = \frac{1}{12L_2}\left(\frac{1}{2^{N_{MSB}}}\right)^2 |(1 - z^{-1})^2|^2_{z=e^{j2\pi k/L_2}}$$
$$S_3(f[k]) = \frac{1}{12L_3}|(1 - z^{-1})^3|^2_{z=e^{j2\pi k/L_3}} \tag{9}$$

Where $L_1$, $L_2$, *and* $L_3$ are the periodicities of quantized noise signals of DDSM modulators of order one to three, which are $2^{N_{LSB}}$ and $2^{N_{LSB}+N_{ISB}}$,$2^{N_{LSB}+N_{ISB}+N_{MSB}}$, respectively.

The error coverage approach is used in this structure, meaning that in order to reduce the quantization noise of the separate line modulator, the noise components $N_1$, $N_2$, and $N_3$ are concealed underneath $N_3$. It is expected that the graphs $S_1$ and $S_2$, which should lie below the $S_3$ curve, are white quantized noise from first- and second-order modulators. There are separate curves here. In a digital Sigma delta modulator with period $L_s$, the lowest frequency tone is at $\frac{f_s}{L_s}$. Therefore, since the periodicity of $N_1$ and $N_2$ is equal to $2^{N_{LSB}}$ and $2^{N_{LSB}+N_{ISB}}$ , respectively, so the lowest frequency tone in the spectrum $N_1$, $N_2$ is equal to $\frac{f_s}{2^{N_{LSB}}}, \frac{f_s}{2^{N_{LSB}+N_{ISB}}}$. Besides, at the output of the modulator, separate nested three-story nested lines 3-2-1, since $S_1$, $S_2$ are formed first and second order, and $S_3$ is formed third order, if the lowest frequency tones $S_1$, $S_2$ are below $S_3$, then all bodies $S_1$, $S_2$ will be below $S_3$. Therefore, (10) can be expressed [17].

$$s_1 < s_3, f = \frac{f_s}{2^{N_{LSB}}}$$
$$s_2 < s_3, f = \frac{f_s}{2^{N_{LSB}+N_{ISB}}} \tag{10}$$

Since

$$|1 - z^{-1}|^2 = \left|1 - e^{\frac{-j2\pi f}{f_s}}\right|^2 = |2\,sin\left(\frac{\pi f}{f_s}\right)|^2, sin\left(\frac{\pi f}{f_s}\right) \approx \frac{\pi f}{f_s} \quad for\ f \ll f_s \tag{11}$$

Therefore, at low frequencies, $S_1$, $S_2$, *and* $S_3$ can be approximated as follows [17].

$$S_1 = \frac{1}{12L_1}\left(\frac{1}{2^{N_{ISB}+N_{MSB}}}\right)^2 2^2.\left(\frac{\pi f}{f_s}\right)^2$$
$$S_2 = \frac{1}{12L_2}\left(\frac{1}{2^{N_{MSB}}}\right)^2 2^4.\left(\frac{\pi f}{f_s}\right)^4$$
$$S_3 = \frac{1}{12L_3}2^6.\left(\frac{\pi f}{f_s}\right)^6 \tag{12}$$

So we have:

$$4N_{LSB} - N_{ISB} - N_{MSB} - 4 < 6.6, 2N_{LSB} + 2N_{ISB} - N_{MSB} - 2 < 3.3 \tag{13}$$

Assuming:

$$N = N_{LSB} + N_{ISB} + N_{MSB}, L = N_{MSB}, M = N_{ISB} + N_{MSB} \tag{14}$$

These equations are expressed as follows.

$$4N - 5M - 4 < 6.6, 2N - 3L - 2 < 3.3 \tag{15}$$

If the input word length is given, $M$ and $L$ can be calculated with (16).

$$M = \left\lfloor \frac{4N-10.6}{5} \right\rfloor, \mathrm{L} = \left\lfloor \frac{2N-5.3}{3} \right\rfloor \quad (16)$$

Therefore, the optimal values for $N_{LSB}$ and $N_{ISB}$, $N_{MSB}$ will be calculated with (17).

$$N_{MSB} = L, N_{ISB} = M - L, N_{LSB} = N - M \quad (17)$$

Similar calculations to determine the appropriate word length of the two-stage modulator, 1-3 separate lines are given in Table I. The following method is performed in order for the three-stage modulator of separate $N$-bit nested lines to have a 1-2-3 structure, and the conventional $N_0$-bit three-layer modulator with the same frequency, and frequency range of $N_0$, the following method is performed. 1- Select $N = N_0 + 1$ to make the output period of the digital Sigma Delta modulator separate lines, similar to the conventional $N_0$-bit multistage modulator.
The optimal structure is selected, and the optimal word length is obtained from Table I.

TABLE I
Optimal Word Length of Sigma Delta Digital Modulator Third-Order Separate Lines

| Sigma delta modulator separate lines | Optimal word length | | |
|---|---|---|---|
| | $N_{LSB}$ | $N_{ISB}$ | $N_{MSB}$ |
| **1-2-3** | $L$ | $M$-$L$ | $N$-$M$ |
| **1-3** | M | | N-M |

A logic gate's hardware cost is half that of a typical CMOS logic circuit, when it comes to transistor count. The hardware expenses of a full adder and a flip-flop D in this architecture are 14 and 4, respectively. Furthermore, the hardware of the second and third DDSM modulators cost for the noise cancellation network are 18 and 55, respectively. For the purpose of implementing the DDSM modulator, the total number of collectors (nFA) and the number of flip-flops D (nFF) are determined as follows:

$$n_{FA(123)} = N_{LSB} + 2N_{ISB} + 4N_{MSB}, n_{FF(123)} = N_{LSB} + 2N_{ISB} + 3N_{MSB} \quad (18)$$

The total hardware consumption of the nested module of separate lines is 3-2-1 equal to (19).

$$HC_{123} = 14n_{FA-123} + 4n_{FF-123} + 55 + 18 = 18N_{LSB} + 36N_{ISB} + 68N_{MSB} + 73 \quad (19)$$

But, the number of all collectors and flip-flops required by the conventional third-order $N_0$ bit modulator is equal to:

$$n_{FA(conv)} = 3N_0, n_{FF(conv)} = 3N_0 \quad (20)$$

Consequently, the normal third-order $N_0$-bit modulator's whole hardware configuration is as follows.

$$HC_{conv} = 14n_{FA-conv} + 4n_{FF-conv} + 55 = 54N_0 + 55 \quad (21)$$

By substituting $N = N_0 + 1$ in the equations, the hardware ratio of two conventional third-order multilayer modulators and the separate nested lines is equal to (22).

$$RHC_{123} = \frac{HC_{123}}{HC_{conv}} = \frac{18N_{LSB}+36N_{ISB}+68N_{MSB}+73}{54N_0+55} \approx \frac{53.4N_0+32}{54N_0+55} \times 100\% \quad (22)$$

This value is reduced by 99% for large $N_0$. Therefore, in multi-layer nested structures 1-2-3 in large $N_0$, hardware consumption is reduced. The hardware-to-hardware ratio of separate two-layer line modules is 1-3 as follows.

$$RHC_{13} = \frac{HC_{13}}{HC_{conv}} = \frac{18N_{LSB}+54N_{MSB}+55}{54N_0+55} \approx \frac{46.8N_0+25.5}{54N_0+55} \times 100\% \quad (23)$$

This value is 87% equal to the large $N_0$s. Therefore, 13% of hardware consumption is reduced. Next, a new structure for the slot is proposed to improve the modulator performance. Fig. 7 shows the proposed oscillator circuit designed using the active inductor.
For increasing the operating frequency of the PFD, a pass transistor logic is added to eliminate the rest path. The proposed PFD has only 10 transistors, which reduces the power consumption and area of the modulator. The proposed structure is shown in Fig. 8.
Fig. 9 shows the noise spectra of the proposed structure and is compared with a conventional one. One can see that the noise is noticeably decreased. The technology used in this paper is 0.18 µm CMOS, and all the papers presented use this technology.

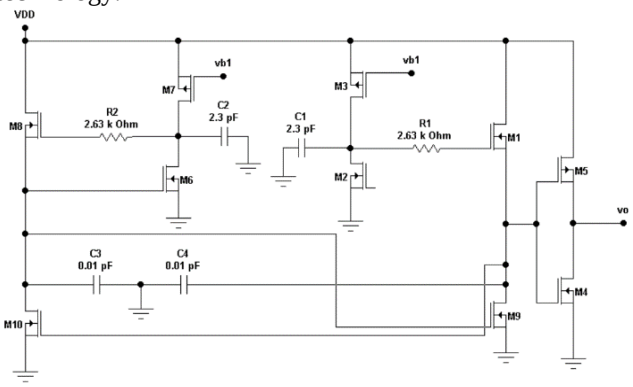


Fig. 7 proposed LC VCO.

In this paper, discrete line technology is used. In this way, a 22-bit fourth-order modulator with 22-bit adder circuits and flip-flops is decomposed and divided into four smaller modulators with 4-4-4-10-bit bits. Therefore, the adder circuits and their flip-flops are smaller, and therefore the power consumption and the number of transistors required to build the circuit are reduced. The proposed multi-stage DDSM modulator circuit has 4-4-4-10 bits, whose power consumption for different transistor models is presented in Table II. The clocked pulse signal frequency of 1 MHz is selected, and the number of transistors in this circuit is 2530 complementary transistors. Table III compares the number of transistors and power consumption of the 1-1-1-1 MASH modulator presented in [11-15] with the proposed method. Fig.10 shows the post-layout of the proposed digital sigma-delta modulator.

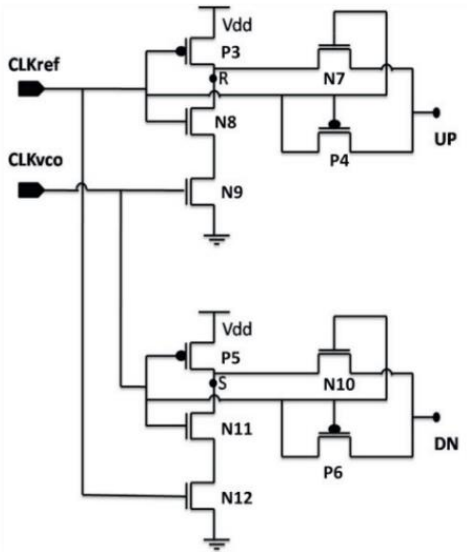



Fig. 8 proposed phase frequency detector (PFD)

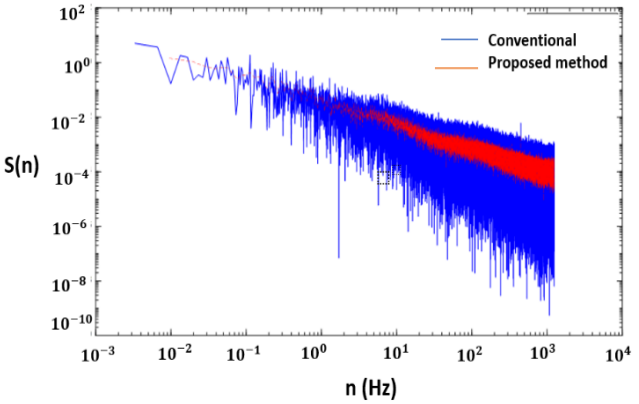



Fig. 9 noise spectra

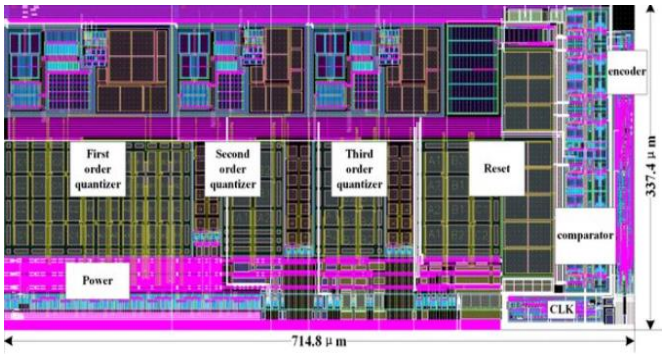



Fig.10: post layout of proposed digital sigma modulator

TABLE II

Comparison of the Power Consumption of the Multi-Stage Modulator Separate of the Proposed Design 4-4-4-10 bits, with the Model of Different transistors N, P.

| Transistor Type | Power Consumption |
|---|---|
| TT | 14.06 nW |
| FF | 75.36 nW |
| FS | 71.09 nW |
| SF | 16.75 nW |
| SS | 110 nW |

TABLE III

Comparison of the Proposed Design with the Methods Presented in [11]-[15]

| Method | Power dissipation | Transistor count |
|---|---|---|
| Proposed method | 131.1619 µW | 2530 |
| Sigma Delta Modulator in [11] | 163.1720 µW | 3420 |
| Sigma Delta Modulator in [12] | 156.23 µW | 2920 |
| Digital Sigma Delta Modulator in [13] | 165.56 µW | 3100 |
| Digital Sigma Delta Modulator in [14] | 161.25 µW | 2950 |
| DDSM in [15] | 159.68 µW | 3250 |

## IV. Conclusions

This research proposes a unique frequency DDSM modulator with fewer components and transistors. The modulator's structure, the initial circumstances, the input, and the quantizer's modulus all affect the quantization noise period. This paper suggests a novel approach for DDSM modulators to lengthen the desired output period while decreasing the spurious tones. The proposed method uses modulators with different word lengths. The input word is divided into several parts, and each part is transferred to a modulator with a shorter word length. Therefore, hardware consumption is reduced, and the power consumption of transistors is reduced. Moreover, in this structure, a dither signal is used to change the alternating state of the output and reduce the spurious tones. The proposed modulator reduces the hardware consumption by 85% compared to the conventional method. Therefore, 15% of hardware consumption is reduced.

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## Conflicts of Interest

The author declares that there is no conflict of interest regarding the publication of this article.

## Authors Contribution Statement

Seyed Ali Sadatnoori: Conceptualization; Numerical Implementation; Experimental Validation; Writing of the Manuscript,

Ghasem Hemmatipour: Data analysis and interpretation; Conceptualization and study design.

## AI disclosure

AI cannot be listed as an author. Only human authors take responsibility.

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