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Design of an LNA Using a Variable Active Inductor with Low Power Consumption for WLAN Applications

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***Abstract*--In this paper, a low-noise amplifier (LNA) using a variable active inductor with low voltage and low power consumption at the load is designed and simulated, which is located in the initial part of an RF receiver. The proposed low-noise amplifier has been investigated to provide low power consumption and suitable noise shaping, compared with other low-noise amplifiers. This circuit is simulated with 180nm CMOS technology, and the results are in the 5.8 GHz frequency range in the WLAN domain. The optimum secondary values for the mentioned elements are obtained from analyses performed using the ADS software. In this circuit, the gain is 20.824, the power consumption is 11.39 mW, and the noise shaping is 2.62 dB. With the addition of inductors with different values within the acceptable range, the calculation of the S-parameters. The S_{11}, S_{12}, S_{21}, and S_{22} are -18.804 dB, -26.155 dB, 20.824 dB and 11.2 dB, respectively. The supply voltage of this circuit is 1.5 V.**

***Index Terms*- Low noise amplifier, variable active inductor, low power consumption, differential pair, Cascode structure.**

I. INTRODUCTION

In recent years, much attention has been paid to wireless communications, and various wireless standards have been developed, and new intelligent radio systems have emerged that can be adapted to various communications. The accuracy of the digital input signal generally limits the performance of digital signal processing systems and communication systems. These systems are considered as the interface between analog and digital information. The low noise amplifier (LNA) is the most important part of a radio receiver. Since it must amplify the low input signal from the receiving antenna to the desired level, and since noise must be kept low because it contributes more to the receiving system's noise figure. Analog-to-digital signal conversion technology based on sigma-delta modulation is a suitable solution for making high-precision converters that are widely used in digital signal processing ICs. The main concept of the sigma-delta modulator is to use feedback to improve the effective accuracy of the internal quantizer. C.C.Culter first proposed this concept. His idea was to measure the quantization error in one sample and subtract it from the next input sample using a delta modulator. Sigma-delta modulation uses the noise shaping concept proposed by Inose, Yasuda, and Murakami in 1962 [1]. A sigma-delta modulator consists of three main components.

a) H(z) loop filter
b) Internal quantizer circuit
c) Digital-to-analog converter in the feedback path.

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In terms of sampling rate, data converters are divided into several categories. 1- Nyquist rate converters 2- Oversampling converters. The sampler converts the analog signal into a discrete-time signal.

This signal is then delivered as an input to the quantizer circuit. This block is the main part of the data converter. In fact, a converter's accuracy is determined by its quantizer's accuracy. The process of converting continuous-time samples of continuous information into a limited number of discrete values is called quantization. Modulators can be single-stage or cascaded.

Various structures have been developed to create an integrated receiver to reduce manufacturing costs and power consumption. This is a critical issue in wireless receivers. Another important issue is the compatibility of the transceivers with different communication standards. Fig. 1 shows the structure of a typical all-digital sigma-delta transmitter. Such a structure uses low-pass sigma-delta modulators operating at a sampling frequency fs to produce two-state outputs vi and vq from in-band data Q and I, respectively. Three multiplexers are then used to digitally amplify the frequency and mix the two-state signals vi and vq together to produce an RF output signal with a center frequency of fc=N.fs.

Merging some blocks in the RF front-end is an effective method to achieve a high integration level and low cost. As shown, a variable gain amplifier (VGA) is inserted between the mixer and the LPF to compensate for the low conversion gain of the mixer and control the signal power level. Consequently, the VGA increases the dynamic range of the DCR. The VGA is typically used along with auxiliary circuits, such as common-mode feedback (CMFB), DC offset voltage cancellation, and the exponential current generator.

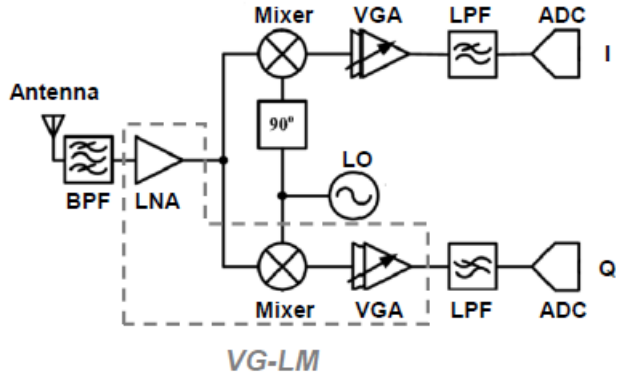

Fig. 1: Direct conversion front-end architecture

A de-interference filter is used to remove the high-frequency components of the input signal to prevent signal degradation in the sampling frequency domain. When the oversampling rate is high, this filter can be very simple and implemented with a simple RC filter, since the sharpness of the filter is of little importance.

Two RF receiver architectures are commonly used in wireless receiver implementations. 1- Direct conversion and 2- Superheterodyne. Superheterodyne receivers reduce the frequency of the input signal from the RF state using two different IF circuit stages. It is preferable to use a filter and an amplifier at each frequency reduction stage. However, this requires two stages of down mixers and two IF filters, which increases the system's power consumption. On the other hand, direct conversion receivers directly convert the RF signal to baseband in a single step. Then, a low-pass filter and amplifiers are used after the mixer. Therefore, direct conversion receivers consume much less power than superheterodyne receivers. However, the structure of these receivers has a DC offset problem that will affect the biasing conditions of the circuits.

Nowadays, there is a growing demand for wireless RF communication systems, making it increasingly important to produce high-performance integrated CMOS products in various parts of RF receiver circuits.

Using the CMOS process in RF systems can reduce power consumption. Since low-noise amplifiers (LNAs) are placed in the first stage of a receiver circuit and are one of the most important building blocks of receiver and transmitter systems, achieving high gain, low noise, good input and output impedance matching, and low power dissipation in them is of great importance. The noise performance of an LNA is largely determined by the system's overall noise performance [5]. Also, the inductor is an important component in the design of impedance-matching networks in LNA design. In addition, implementing a passive helical inductor on the chip is difficult; on the other hand, using an active inductor provides a large amount of inductance with a high resonant frequency, high quality, and a small chip area. The active inductor can be used at the input of the matching network or on the load side [12]. In this paper, an active inductor is designed and optimized for use in a low-noise amplifier in the WLAN domain, reducing noise and power consumption. The structure of this paper is as follows. Section 2 presents the design of the active inductor. Section 3 describes the low-noise amplifier. Section 4 presents the simulation results, and the last section is the conclusion.

II. Active Inductor Design

The proposed single-ended active inductor uses the gyratory-C structure [8], which converts the inherent capacitance of the circuit into inductive behavior and is shown in Fig. 2. This circuit consists of a differential pair M1 and M2, which represents a positive voltage-to-current converter G_{m1} between the input (node 1) and the output (node 3). Also, in this circuit, a cascade section consisting of transistors M3 and M4 is located between the input (node 3) and the output (node 1), which represents a negative voltage-to-current converter -G_{M2}. Thus, G_{m1} and -G_{m2} represent a gyratory form in which the parasitic capacitor C_3 at node 3 is converted into an equivalent inductor $L_{eq} = \frac{C_3}{G_{m1}G_{m2}}$ [14]. The proposed active inductor is fabricated using a PMOS cascade structure. It acts as a negative voltage-to-current converter, which can lead to a possible negative series resistance and can be used to compensate for inductor loss. Therefore, p-channel transistors were used for the cascade structure [3], which, in addition to low noise, can be placed in separate n-wells, thus eliminating the nonlinear body effect. Therefore, the quality factor of the active inductor is increased, and the resonant frequency is higher, and the bandwidth is better [9].

To further improve the quality factor, the series resistance Rs should be reduced. Therefore, transistor M5 can be used between the positive voltage-to-current converter and the negative voltage-to-current converter in the active inductor.

The M5 transistor acts as resistive feedback, increasing the loop gain and the quality factor of the active inductor. Transverse conduction in the transistor is achieved by controlling the V_{GS} source at the gate of transistor M5 [2]. In the designed active inductor, by varying the V_{GS} of transistor M5, the operating frequency of the circuit can be changed, creating a variable active inductor.

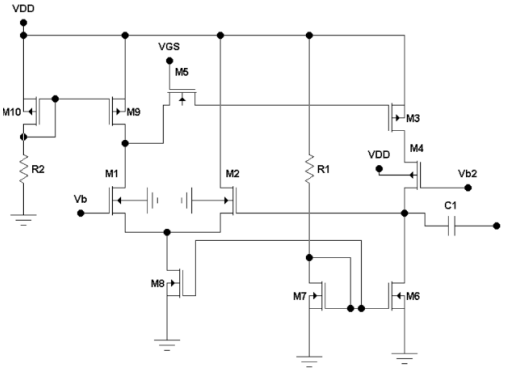

Fig. 2: Single-ended active inductor circuit diagram

For example, by setting V_{GS} = 0.17 V, the operating frequency is 6.1 GHz, and by increasing it to V_{GS} = 0.63 V, the operating frequency changes to 5.5 GHz, which shows the flexibility of the circuit in the frequency domain. Also, by designing transistor M2, the noise generated is reduced [13]. The input impedance of the active inductor circuit is equivalent to zin, which is obtained from the small-signal analysis of the circuit with (1). (Fig.3)

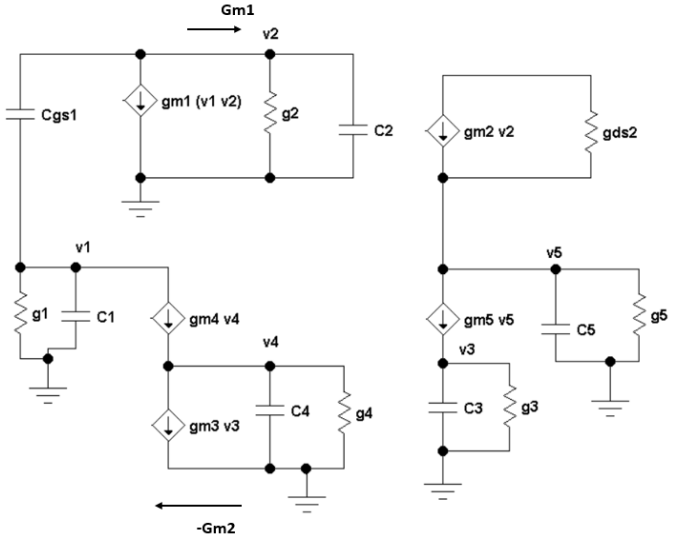

Fig. 3: Small signal diagram of a single-ended active inductor circuit.

$$z_{in}(s) = g_1 + sC_1 - \frac{g_{m5}g_{m4}g_{m3}g_{m2}g_{m1}}{(G+sC_2)(g_3+sC_3)(g_{m4}+g_4+sC_4)(g_{m5}+g_5+sC_5)} \quad (1)$$

In (1), $G = g_{m1} + g_{m2} + g_2$ is considered.

The z_{in} equation shows that the active inductor circuit is equivalent to a parallel RLC network, as shown in Fig. 4. [10] By analyzing the circuit in Fig. 3, the equivalent inductance and series resistance of the active inductor can be obtained.

$$L_{eq} = \frac{C_3 G g_4 g_5}{g_{m5}g_{m4}g_{m3}g_{m2}g_{m1}+Gg_1g_3(g_{m4}+g_4)(g_{m5}+g_5)} \quad (2)$$

$$R_s = \frac{C_3 g_3 g_4 g_5}{g_{m5}g_{m4}g_{m3}g_{m2}g_{m1}+Gg_1g_3(g_{m4}+g_4)(g_{m5}+g_5)} \quad (3)$$

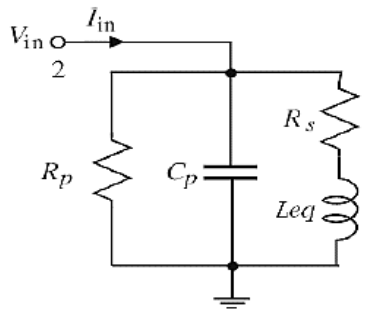

Fig. 4: Active inductor RLC equivalent circuit

The parallel capacitor $C_P = C_1$ and the parasitic parallel resistance $R_P = \frac{1}{G_2}$, as well as the resonant frequency ω_0 and the quality factor Q_0 are obtained as follows.

$$\omega_0 = \sqrt{\frac{g_{m5}g_{m4}g_{m3}g_{m2}g_{m1}+Gg_1g_3(g_{m4}+g_4)(g_{m5}+g_5)}{GC_1C_3}} \quad (4)$$

$$Q_0 = \frac{\sqrt{\frac{g_{m5}g_{m4}g_{m3}g_{m2}g_{m1}+Gg_1g_3(g_{m4}+g_4)(g_{m5}+g_5)}{GC_1C_3}}}{[\frac{g_1}{C_1}+\frac{C_2g_1g_3}{GC_1C_3}+\frac{g_3}{C_3}-\frac{\omega^2C_2}{G}]g_4g_5} \quad (5)$$

A. Calculation of the power consumption of an active inductor

To calculate power consumption, we must first obtain the constant voltage and current for each circuit branch. In the active inductor, the entire circuit is powered by a 1.5 V battery. In the proposed active inductor circuit, two current mirrors are used. The current of the current mirror of M6 and M7 is equal to 0.18 mA, and the current of the current mirror of M9 and M10 is equal to 0.12 mA. Also, the current of the transistor branch m2 is also equal to 0.01 mA, which means that the total current of the active inductor is equal to:

I_P=0.12 mA + 0.18 mA + 0.01 mA = 0.31 mA (6)

The power consumption is obtained from (7). This power consumption shows that the proposed active inductor consumes low power.

$$P = V.I_P = 1.5\ \text{V} \times 0.31\ \text{mA} = 0.465\ \text{mW} \quad (7)$$

B. LNA amplifier circuit structure

The structure of the LNA circuit is shown in Fig. 5 [7]. This amplifier uses a common-source amplifier as well as a passive inductive load, and two common-drain circuits to match the input and output impedances to a 50-ohm resistor. The gain of this common drain circuit is less than zero dB, and the output impedance of the common drain circuit is defined as $\frac{1}{g_m}$.

RC feedback is used to match the input impedance. The cascade amplifier generally forms the core of the LNA circuit.

This circuit has a high output impedance and low noise due to the Miller effect in the input device. Therefore, it is more suitable for design compared to other amplifier circuit topologies [6]. In Fig. 4, RF is a feedback resistor used to achieve 50-ohm input impedance matching, and C_F is used to match the input at high frequencies and to improve the frequency response of the amplifier [15]. Fig. 5 shows the LNA circuit with an active inductor load. In this circuit, the inductance of the active inductor is obtained based on the value of V_{GS} in the transistor M5, and the inductance of the inductor

changes with changes in V_{GS}. At low frequencies, the input impedance of the LNA is equal to $Z_{in} \approx R_{IN}$. Also, transistor M1 significantly affects the noise value, which decreases with increasing G_{M1} [11].

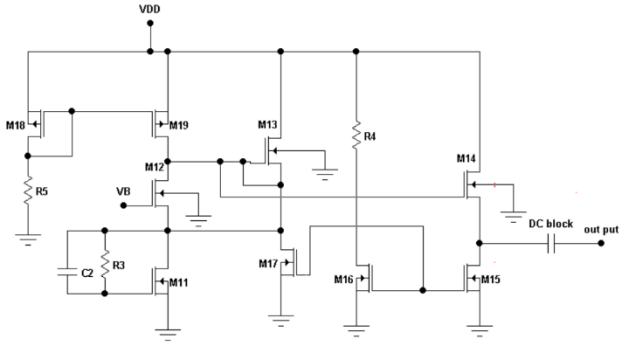

Fig. 5: LNA circuit block diagram

$$Z_{in} = \frac{1}{sC_{gs1} + \frac{g_{m3}}{1+Z_F g_{m3}}\left(1+\frac{g_{m1}g_{m3}Z_L}{g_{m2}}\right)} \quad (8)$$

$$R_{in} = \left(R_F + \frac{1}{g_{m3}}\right).\left(\frac{g_{m2}}{g_{m1}+g_{m2}}\right) \approx R_F.\left(\frac{g_{m2}}{g_{m1}+g_{m2}}\right) \quad (9)$$

Where, g_{m1}, g_{m2}, and g_{m3} are the voltage-to-current converters of transistors M1, M2, and M3 [4].

To calculate the total power consumption in the amplifier circuit, we first calculate the total current, which is 7.23 mA. Then the product of the voltage and the total current is the total power consumption of the circuit, which is as follows:

$$P_{LNA} = 1.5\ \text{V} \times 7.23\ \text{mA} = 10.845\ \text{mW} \quad (10)$$

$$P_{Total} = P_{LNA} + P_L = 10.845 + 0.37 = 11.39\ \text{mW} \quad (11)$$

The complete circuit of a low-noise amplifier with an active inductor is shown in Fig. 6. The values of the resistors and capacitors and the circuit supply voltages are selected as shown in Table I.

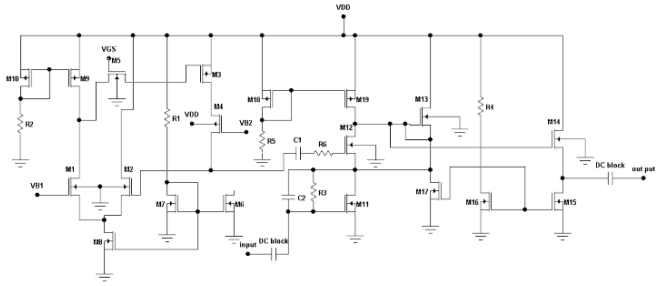

Fig. 6: Block diagram of the proposed low noise amplifier circuit with an active inductor.

III. Simulation Results

S-Parameter Simulation Results. Using ADS, the suggested LNA is developed and simulated in the RF-TSMC CMOS 0.18 μm technology. We applied the existing ADS optimization algorithm. We may establish our targets, the type of optimization, and eventually the range of the required optimized parameters using this approach. Using the ADS software, the effects of any increase or decrease in the output matching circuit elements, i.e., the inductor and capacitor, can be observed. In this circuit, the effects of process corners and parasitic effects are not modeled.

The results of the transmission gain S_{21}, S_{11}, S_{12}, and noise in the low-noise amplifier circuit with an active inductor are shown in Figs. 6-10 for the center frequency of 5.8 GHz. Also, in Table II, the values obtained from this design are compared with those from some previously used methods, demonstrating the appropriate quality of this amplifier circuit compared to other circuits.

TABLE I
Values of the Parameters of the Elements in Fig. 6

Parameter name	Value
V_{DD}	1.5 V
V_{b1}	0.2 V
V_{GS}	0.3 V
V_{b2}	137 mV
R_1	13 KΩ
R_2	1.5 KΩ
R_3	0.9 KΩ
R_4	250 Ω
R_5	5 KΩ
R_6	100 Ω
C_1	0.5 pF
C_2	0.6 pF

In the proposed method, the circuit gain is 20.854, which is higher than that of other methods. Also, the power consumption in the proposed circuit is calculated to be 11.39 mW, which is lower than that of other methods.

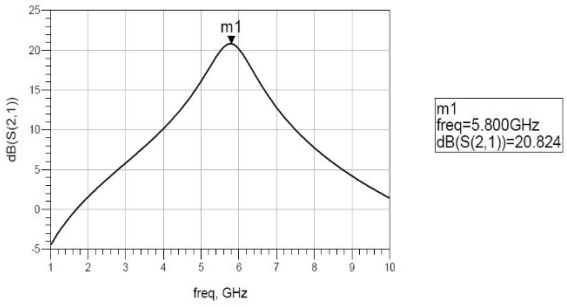

Fig. 7: Parameter S_{21} in the complete LNA circuit with an active inductor at 5.8GHz frequency

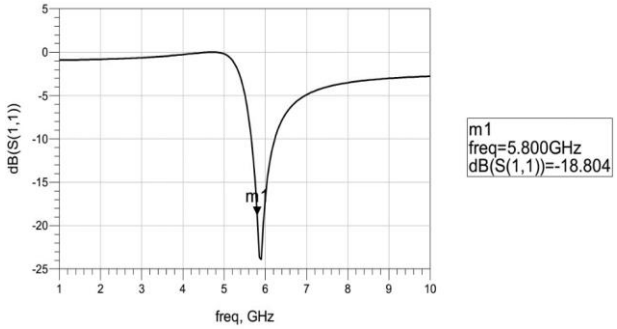

Fig. 8: S_{11} parameter in the complete LNA circuit with an active inductor at 5.8 GHz frequency

Fig. 11 shows the noise-shaping values for the operating frequency of 5.8 GHz. As shown in this figure, at 5.8 GHz,

frequency bands were designed with a maximum noise figure of 2.62 dB and a minimum gain of 20.854 dB.

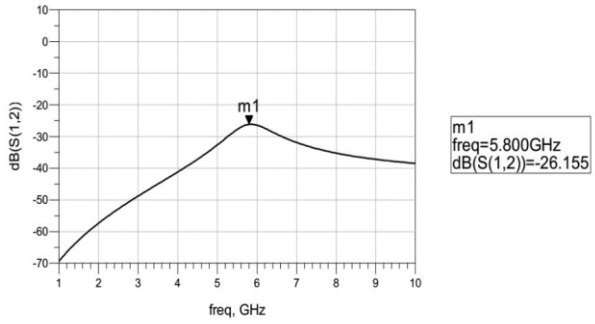

Fig. 9: S_{12} parameter in the complete LNA circuit with an active inductor at 5.8 GHz frequency.

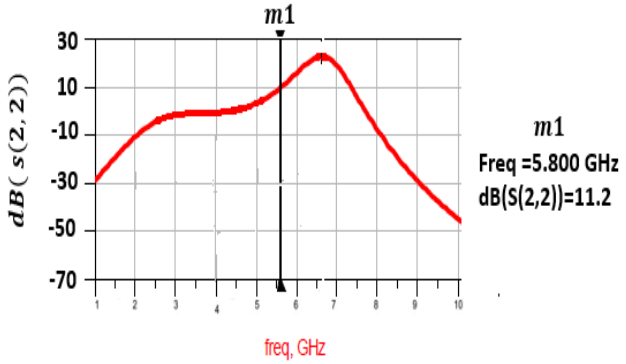

Fig. 10: S_{22} parameter in the complete LNA circuit with an active inductor at 5.8 GHz frequency.

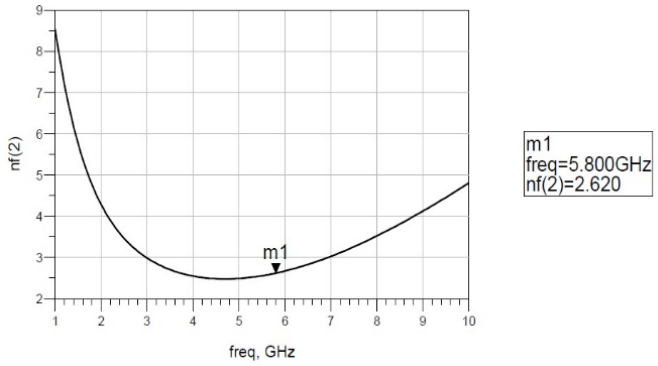

Fig. 11: Noise parameter in the complete LNA circuit with an active inductor at a frequency of 5.8 GHz.

In this paper, harmonic balance simulation is used to investigate the LNA. Two input tones with the same power but a very close frequency separation are used to calculate the distortion product between the modulation and the third-order cutoff point. At different frequencies, these two tones combine, producing distortions at higher frequencies. As shown in Fig 12, the value of the IIP3 point is equal to -26.5 dbM, indicating good linearity for such a nonlinear device.

The figure of merit (FoM) is calculated as per the following expression [2].

$$Fom = \frac{Gain}{(NF-1)\times P_{dc}} \quad (12)$$

For this amplifier, the maximum noise figure is 2.62 dB, and the minimum gain value is 20.854 dB. The P1dB parameter simulation results for the first and second frequency bands are shown in Fig. 13.

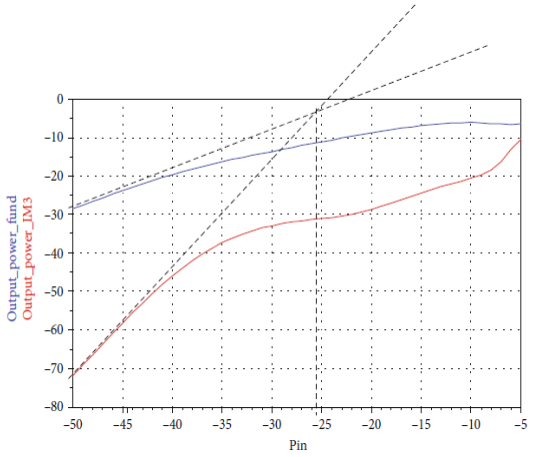

Fig. 12: Simulated IIP3 of the proposed circuit

TABLE II
Comparing the Obtained Results with Previous Results

Refer	S. Heydarzadeh, M. Dousti [3] [2012]	Mohsen Moezzi et all [9] [2012]	Mahbub Reja, et all [4] [2008	JIN-FA CHANG [7] [2025	A. Bijari [11] [2024]	Proposed method
Tech	0.18 µm	0.13 µm	0.13 µm	0.09 µm	0.13 µm	0.18 µm
Volt	1.8 V	1.2 V	1.5 V	1.2 V	1.2 V	1.5 V
Amp	20	11.8	11.8	11.8	14.18	20.824
Noise	2.7-3.6	1.9-3.8	2-4	3.1-4.4	2.44	2.62
Power	19.6 mW	13.3 mW	13.5 mW	16 mW	8.79 mW	11.39 mW
IIP3	27.8	-	-	-9.3	-10.4	-26.5
Freq	2.5 GHz	1.8-12.4 GHz	2-11.2 GHz	3-8.5 GHz	2-4 GHz	5.8 GHz
Fom	-1.02	2.37	-	1.677	2.88	41.57

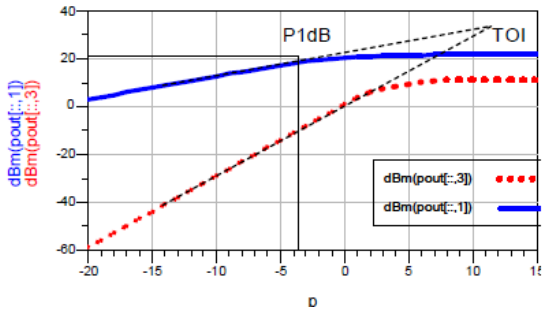

Fig. 13: The P1dB parameter simulation results for the first and second frequency bands.

Stability is analyzed using Eqs. (13) and (14). The results of the stability analysis show that, because k>1 and δ<1 are not obtained, this transistor is not stable in the S-band frequency range. One way to stabilize is to insert an inductor at the transistor source. With the addition of inductors with different values within the acceptable range, the calculation of the S-

parameters. Fig. 13 shows the values of K versus frequency after stabilizing the transistor.

$$K = \frac{1-|s_{11}^2|-|s_{22}^2|+|\Delta^2|}{2\times|s_{21}.s_{12}|} \quad (13)$$

$$\Delta = s_{11}.s_{22} - s_{21}.s_{12} \quad (14)$$

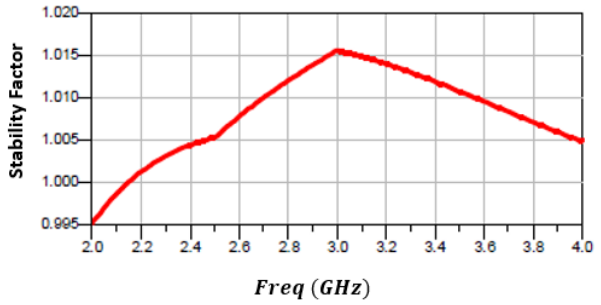

Fig. 13: K values after stability.

The measured stability factor μ in Fig. 14 indicates that the circuit is unconditionally stable between 0–9 GHz. [8].

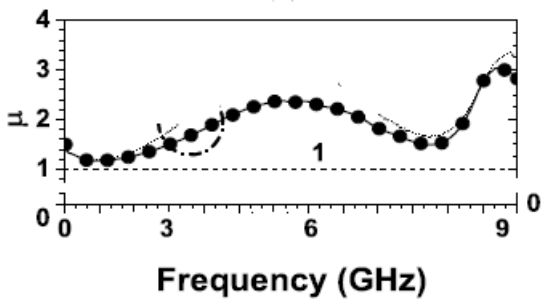

Fig 14: The measured stability factor μ in the proposed method.

In [13], a low-power active inductor for WLAN telecommunication applications is presented. In this reference, the sampling frequency is 5.5 GHz. In this reference, the values of the parameters s11, s12, and s21 are -14.15, -21.8, and 21.7, respectively. The noise factor value in this reference is 1.6. In the proposed circuit, the noise shaping value is better, and the values of the S parameters are more optimal.

IV. Conclusion

The presented work describes a low-power WLAN LNA for WSN wake-up receiver applications. In this paper, the LNA configuration is presented based on AI design. This paper is implemented with 0.18μm CMOS technology. Among the advantages of this active inductor are flexibility in selecting the frequency band, low power consumption, and a small chip size. Also, the results obtained in this paper at a frequency of 5.5 GHz include S_{21}=20.824 dB, S11=-18.802 dB, S12=-26.155 dB, S22=11.2 dB, and NF=2.62. Also, the working voltage of the circuit is 1.5V.

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Conflicts of Interest

The author declares that there is no conflict of interest regarding the publication of this article.

Authors Contribution Statement

Seyed Ali Sadatnoori: Conceptualization; Numerical Implementation; Experimental Validation; Writing of the Manuscript,

Ghasem Hemmatipour: Data analysis and interpretation; Conceptualization and study design.

AI disclosure

AI cannot be listed as an author. Only human authors take responsibility.

Data availability

All data generated or analyzed during this study are included in this published article.

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