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An Efficient Approximate Vedic Multiplier Circuit Design by Bit-Slicing Method Based on QCA Technology

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***Abstract*-- Nowadays, due to the ubiquity of portable electronic equipment and their limited battery charge, low-power circuit design based on compression has been one of the biggest criteria for researchers, which will create some limitations and challenges. However, one way to reduce power consumption is to use approximate units based on quantum cellular automata technology in systems. In this study, we design an approximate multiplier using quantum cellular automata technology. Using the full-adder design scheme to obtain partial multiplications and place them in a particular arrangement, we arrive at an approximate multiplier. The proposed design can improve on quantum costs (53%), constant inputs (15%), and Area (55%). In addition, it is shown that the QCA technology is effective for implementing complex computational circuits and can provide a good performance over a precise circuit. The design and the simulation of the circuits in this study have been performed using the QCA Designer tool version 2.0.3.**

***Index Terms*- Quantum dot cellular automata, Quantum computing, QCA approximate multiplier, approximation calculations, low-power circuit design, very compact quantum circuits.**

I. INTRODUCTION

With advances in technology, digital systems require heavy processing and increased power consumption, making power consumption a critical parameter in their design. Important problems in CMOS technology include high power consumption, noise absorption, and high implementation costs, making it difficult to build high-speed, low-power, and easy-to-build VLSIs. In recent years, desirable advances have been made in manufacturing processes, design techniques, and computational methods to reduce the power dissipation of circuits [1]. The major part of power consumption in digital circuits is dedicated to arithmetic operations [2-4]. Also, according to Moore's law, doubling the number of transistors every 18 months encounters this process with physical challenges and limitations, especially at the nanoscale [5]. Quantum-dot Cellular Automata (QCA) is considered a promising beyond-CMOS technology due to its ultra-low power consumption and high device density. However, several practical challenges, including fabrication complexity, thermal stability, and defect tolerance, must be addressed before large-scale implementation. [7].

On the other hand, in the 1960s, Landauer showed in his research that irreversible classical circuits, regardless of the technology used for construction and implementation, dissipate information in the form of heat [6]. This fact threatens the improvements in practical computer performance within the next few decades. However, the power dissipation of computations based on reversible logic operations (computations for which every possible output state comes from exactly one input state) can approach arbitrarily near zero.

One of the most important arithmetic circuits is the multiplier. Fig. 1 shows the structure of a multiplier, which typically consists of three phases: the initial phase, the production of partial multiplications, the second phase, the sum of the partial multiplications, and the final phase, the sum of two final vectors, which can be approximated in any of the phases.

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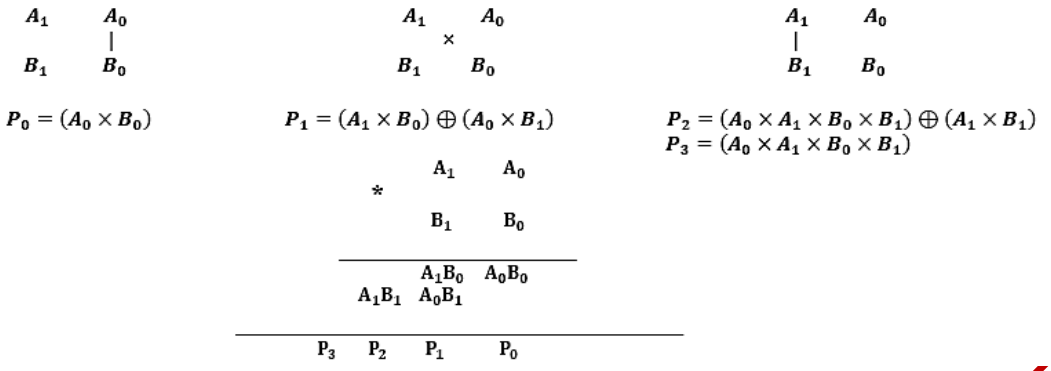

Fig. 1. The multiplier structure.

The approximation may be applied during the phase of production of partial multiplications. In studies [8] and [9], the number of partial multiplications has been reduced. Also, in [8], half of the number of bits of operands has been removed, and in [9], the most valuable bit is recognized, and the number of bits after that are considered as operands. In some methods, approximation is used to sum partial multiplications. In [10] and [11], approximately 4:2 compressors have been used, and in [12], approximate full-adders have been used for the addition of partial multiplications. The delay and power consumption are greatly influenced by the final phase, i.e., the sum of the final vectors. For this reason, approximate adders have been used in [13]. In [14] and [15], multiplication is performed by changing the display of operands. In [14], operands are expressed logarithmically so that multiplication can be performed by addition. In the paper [15], by rounding the numbers and approximating them to the nearest value, multiplication is performed by only a small number of additions and shifts.

The study in [16] used the parallel-serial multiplier method and the majority gate to improve the design values to a desirable level. The study in [17] used a systematic algorithm to improve processing speed and reduce the number of gates. In [18], a serial full adder method with a delay coefficient was used. In [19], the first multiplier is designed using reversible logic. Also, the study in [20] uses the same method and the large reversible gate to reduce the number of gates, complexity, and quantum cost. In [21], a multiplier with an error-protection property is proposed using three gates, ZPl, ZQC, and ZC, thereby reducing the number of gates and quantum cost. The sum of the partial multiplications is used to approximate the propagation of a shorter transport figure. In the study [22], a full adder with a carry bit is proposed using the unique features of QCA. The study [23] mentions the use of multipliers and reviews 100 papers from 2015 to 2020 to improve the implementation and design parameters.

Nowadays, power consumption within chips is relatively limited, and approximate calculations have been able to replace precise circuits by shortening the critical path. Approximate computational circuits enable optimizing circuits for applications that do not require precision by making the right compromise between power consumption, latency, and output accuracy [24-29]. Many studies have been published in the field of approximate addition, and several approximate adders have been proposed to approximate the least significant output bit [30-33]. Unfortunately, these methods require the design of specific standard cells, and their statistical accuracy is adjusted during design, which is a significant limitation because the quality of execution depends on the settings at the time of design [26, 34]. In fact, it statically regulates accuracy and may not be able to meet output quality or unnecessarily increase power consumption under normal circumstances. For this reason, adders should be designed within automated frameworks that adjust the approximation level based on user demand [9, 35]. In particular, the bit-slicing scheme was introduced to inhibit the activity of LSBs by setting the input bits to zero. However, this method shows that by slicing larger bits, a suitable power reduction can be obtained, as shown in Fig. 2, how to slice bits [31, 36].

By slicing the bits in the LSB parts and zero considering the values in Fig. 2, it was shown that in a) the difference between the precise and the approximate summation is 312, which is a relatively

large number, so in part b, by replacing these bits with an approximate sum of values, the difference of the obtained result with the exact value is 57, which is close and acceptable.

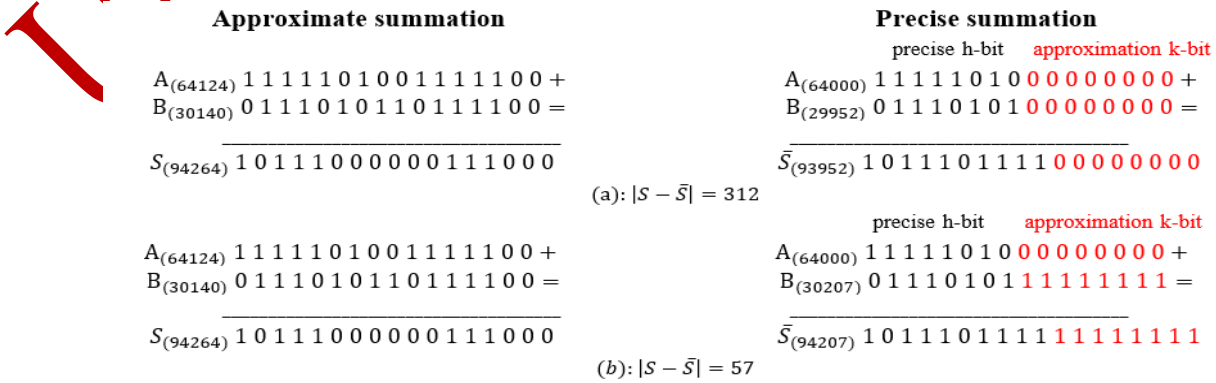

Fig. 2. Approximate adder structure
bit-slicing by the traditional method (b), an example of the proposed method in [37].

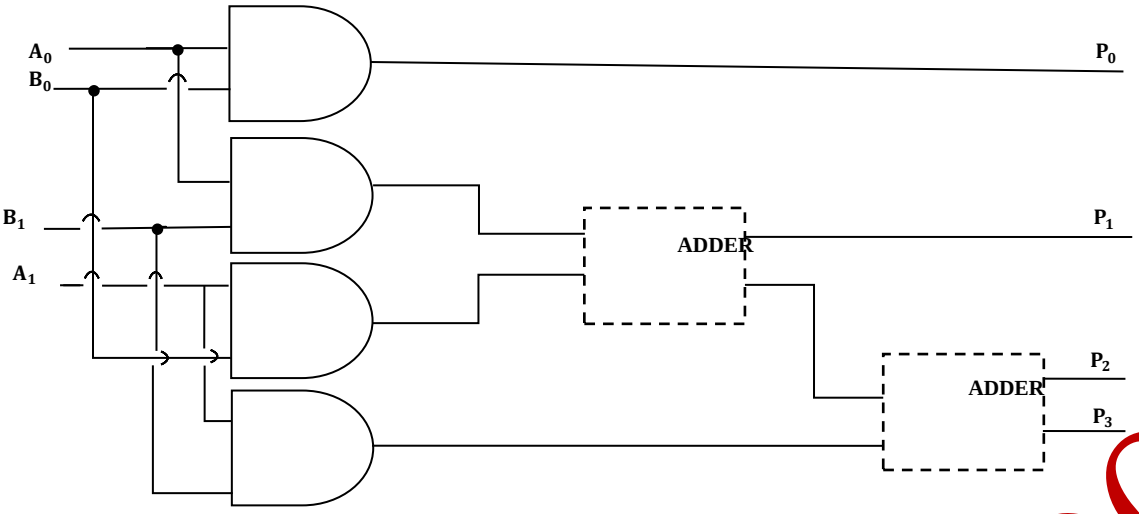

Fig. 3. The multiplier circuit structure.

In [37], a summation is presented that can be used to add the results of partial multiplications with changes and obtain the final multiplication with the result of partial multiplications produced. In fact, the collectors' inputs result from minor shocks. The structure of the collectors in multiplication is shown in Fig. 3.

To design the circuit of Fig. 3 using the model of Fig. 2, instead of zeroing and uniting the k-bit values that are the approximate values in the bit section, we fill their input values with an approximate value so that the inputs in this part pass through the gate and are controlled by signals C0 and C1. These signals work in such a way that, for example, if zero is given to C0, zero is ineffective in the OR gate, and C becomes one, which has no effect on the AND gate and causes us to obtain an exact answer in the output. However, if the input is 1, it affects both gates. If the inputs A and B have any values, the output of the OR gate is equal to one, the output of the AND gate is zero, and it is given to the full-adders. In the full-adder part, a three-input XOR gate and a five-input MAJ function are designed, and we use the obtained AND gate and the full-adder in the design of the multiplication structure of Fig. 3, which is the structure of a 2 × 2 multiplier. As mentioned, we can achieve a higher level of multipliers by combining a few base 2 × 2 ones.

The main contributions of this work are as follows:

• A circuit-level approximation methodology is proposed, where approximation is introduced within full-adder units used for partial product accumulation, instead of applying truncation at the operand level. This leads to a different error propagation behavior.

• Two QCA-compatible logic structures, namely MKN1 and MKN2, are proposed. These structures are optimized for majority-gate realization and reduce logic depth and cell count compared to conventional QCA mappings.

• A hybrid approximate multiplier architecture is developed by integrating the Urdhva Tiryakbhyam Vedic multiplication algorithm with selective approximation applied to lower-significance computation paths.

• A comprehensive evaluation is performed using exhaustive simulation over all 256 input combinations, including hardware metrics (cell count, area, delay) and accuracy metrics (ER, NMED, and MRED).

The remainder of this paper is organized as follows. In Section II, the literature review is mentioned. In Section III, the proposed approach is introduced. In Section IV, the implementation results and comparisons are given, and finally, Section V concludes the paper.

II. LITERATURE REVIEW

Power consumption includes two components, dynamic and static. Leakage currents and short circuits are called static power, while switching modes are called dynamic power. To reduce power, one main technique is signal reduction, which uses the data-gating technique. In this technique, changes to the input status are not transmitted to the full adders; the output is determined separately, using less hardware. In that case, switching power will be reduced, information will be lost, and the error increases. A new computational model is a quantum cellular automata that encodes binary information in cells rather than in conventional switches. Coulombic interactions between electrons are sufficient for computations, and there is no current between the cells, making them a possible solution for transistor less computations with a reduced power consumption at the nanoscale.

QCA has a square structure consisting of four quantum dots and two electrons. Coulombic interactions cause electrons to occupy the two opposite corners of the cell, making polarizations of 1 and -1, which are equivalent to binary values of 1 and 0, respectively, which is the standard display at 90 degrees [38].

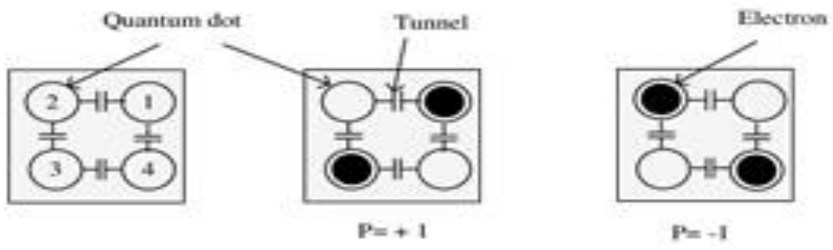

Fig. 4. Quantum cellular automata cell structure in the standard mode.

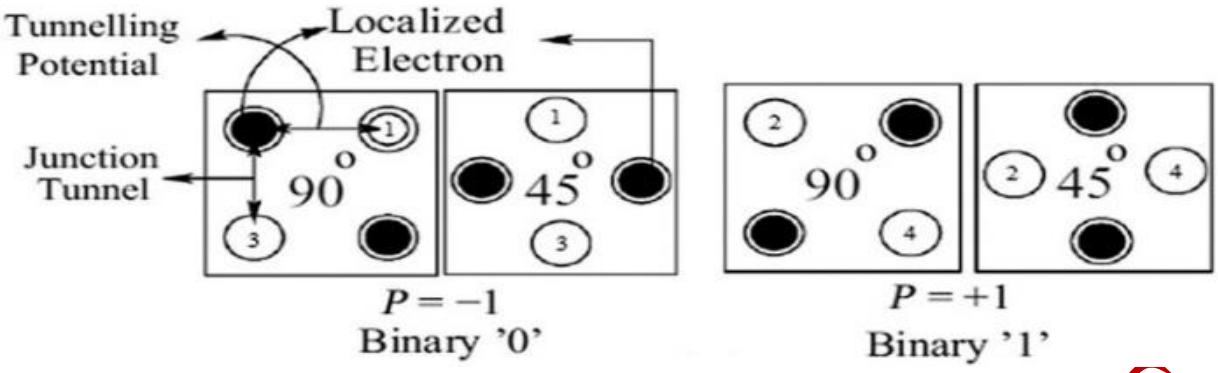

Fig. 5. Quantum cellular automata cell in 45- and 90-degree rotation.

Other forms include the 45-degree structure, in which one cell rotates 45 degrees and the other 90 degrees clockwise.

To transfer information from one cell to another, a binary wire can be seen as a horizontal sequence of cells. An example of a wire is shown in Fig. 6, which is sequentially from 90° cells (Input (blue), data transfer (green, purple, blue, white), and the output (yellow)). This binary wire is divided into different clock regions to prevent the main signal from degrading into declining signals along a long chain of cells within the same timing region [39].

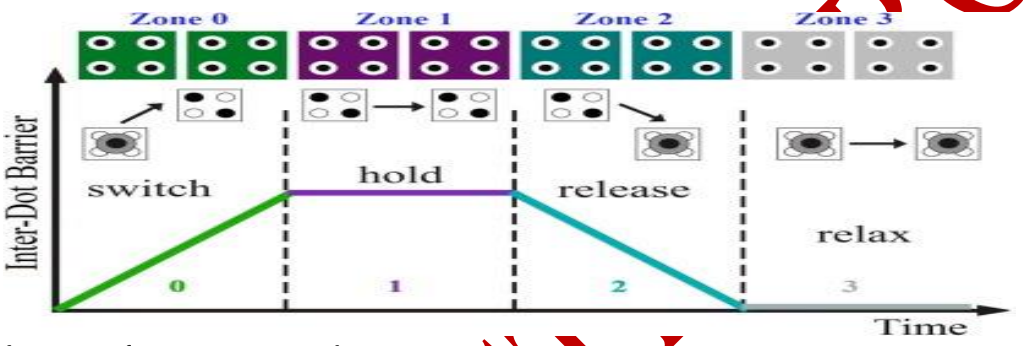

Fig. 6. 90-degree wire information transmission chain.

The signal propagation of 45-degree cells is different. As shown in Fig. 7, due to Coulombic interactions between adjacent cells, they have opposite binary values; hence, it is called the inverse chain, and the amount of data depends on the length of the wire.

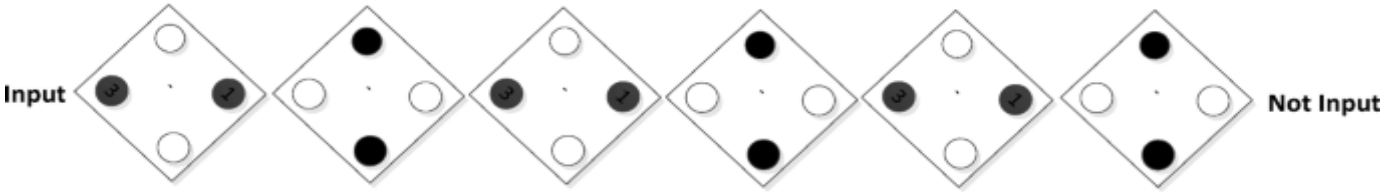

Fig. 7. 45-degree wire structure.

If one of the inputs takes the value 1, according to Table I and Fig. 8, the gate output equals the result of the OR operation of the other two inputs. If one of the inputs is set to zero, the gate output is equal to the result of the AND operation of the two other inputs.

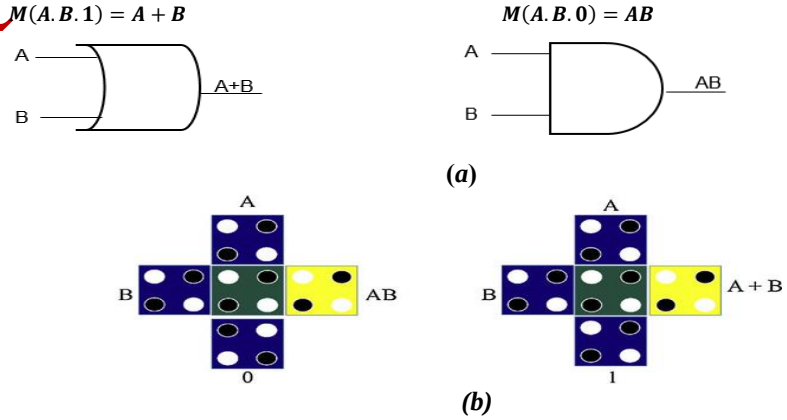

Fig. 8. (a) The structure of OR and AND gates, (b)The implementation in QCA.

The block structure of the majority gate in the logic of the quantum cellular automata is shown in Fig. 9. The data are the same in one clock phase because, until they reach the majority gate, the majority gate function is correctly performed. The majority is applied to the number of inputs in the output according to Table I [7].

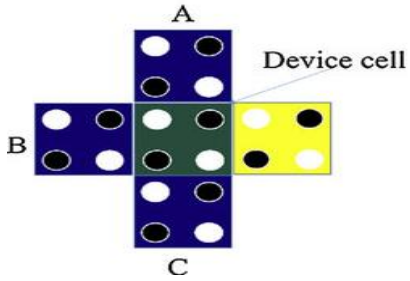

Fig. 9. The majority gate structure.

Fig. 10. The majority gate simulation.

TABLE I

The Truth Table of the Majority Gate.

A	B	C	M (A, B, C)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

III. The proposed approach

The multiplication is done in the form of Urdhva Tiryagbhyam Sutra, which means "vertical and cross", and the product of partial multiplication is added together to get the final result. The base of multiplication is on 2 × 2, and its repeated arrangement can achieve n-bit multiplication. Therefore, calculations are performed very quickly because they require fewer steps [40]. The Vedic multiplication method is described in five steps, as shown below and in Fig. 1.

Step 1: The least significant bits of these two numbers are multiplied to form the (vertical) LSB result.

Step 2: The next higher bits are multiplied together, and the results are added to compute the next digit.

Step 3: The transport part of Step 2 is added to the output of the next level surface to compute the next higher bit.

Step 4: All bits are processed in the same way as Steps 2 and 3 to compute the last digit of the operand.

Step 5: The final product of Vedic multiplication is obtained.

The 4-bit multiplier module (VM) is built using four 2-bit multiplication units, three 4-bit carry adders, and a half-adder gate added as shown in Fig. 11. Inputs A_i (A_3 A_2 A_1 A_0) and B_i (B_3 B_2 B_1 B_0) are specified by a 2-bit Vedic multiplier, and then the multiplier output is sent to the 4-bit RCA adder. The output of the RCA add-on consists of 4 bits of the sum output and a 1-bit overflow. The half-adder is used to add the overflow value in the first RCA. The 4-bit multiplication output consists of the 8-bit multiplication (P_i - P_7 … P_0) terms [40].

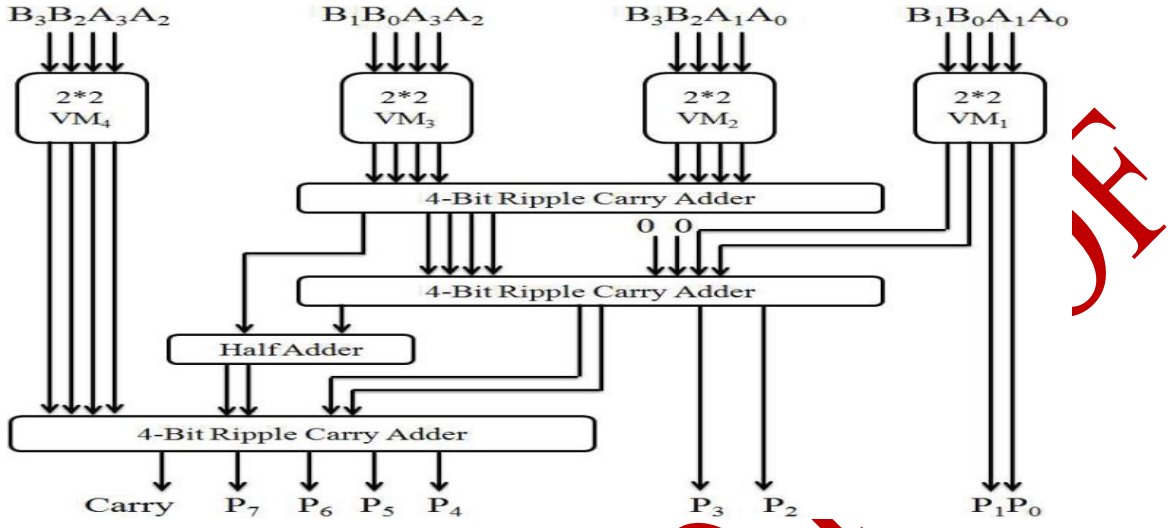

Fig. 11. The structure of a 4-bit multiplier hardware.

In a similar method, the Vedic multiplier with a higher number is produced by 2-bit VM_is made as the base module and the RCA full-adders for the partial overflows. An n-bit multiplier is created by dividing the number of bits (n) by the base of the multiplier, which is 2 (n/2). In other words, it will generally consist of an RCA adder, an n-bit full adder, and a [(n / 2) −1]-bit RCA half-adder. For example, to build a 16-bit multiplier with this structure, four 8-bit multiplication units, a 16-bit RCA adder, a 16-bit adder, and a 7-bit RCA half-adder are required. The construction of the general n-bit multiplier is shown in Fig. 12.

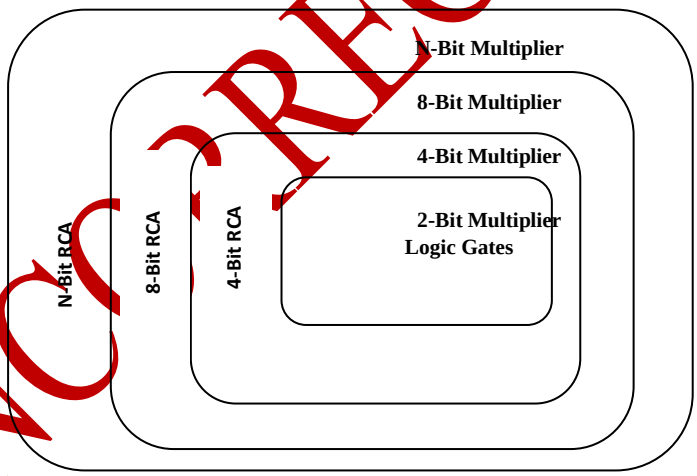

Fig. 12. The overall structure of the n-bit multiplier.

IV.IMPLEMENTATION AND COMPARISON

The proposed design is based on the paper [41], which is to calculate the sum of the product of partial multiplications, and with the help of MKN1 and MKN2 gates, we obtain the final outcome of the multiplication. In fact, the product of partial multiplications is the input of the full-adders. This is an approximate 8-bit full-adder whose circuit is divided into two parts, and the calculations are performed in two parts, precise and imprecise. An approximation of the sum of n bits is generally computed by dividing it into a precise h-bit fraction and an imprecise k-bit, with n = h + k. This design is based on the approximate XOR of the three inputs of Fig.13, using which the design of an approximate 8-bit full-adder is obtained.

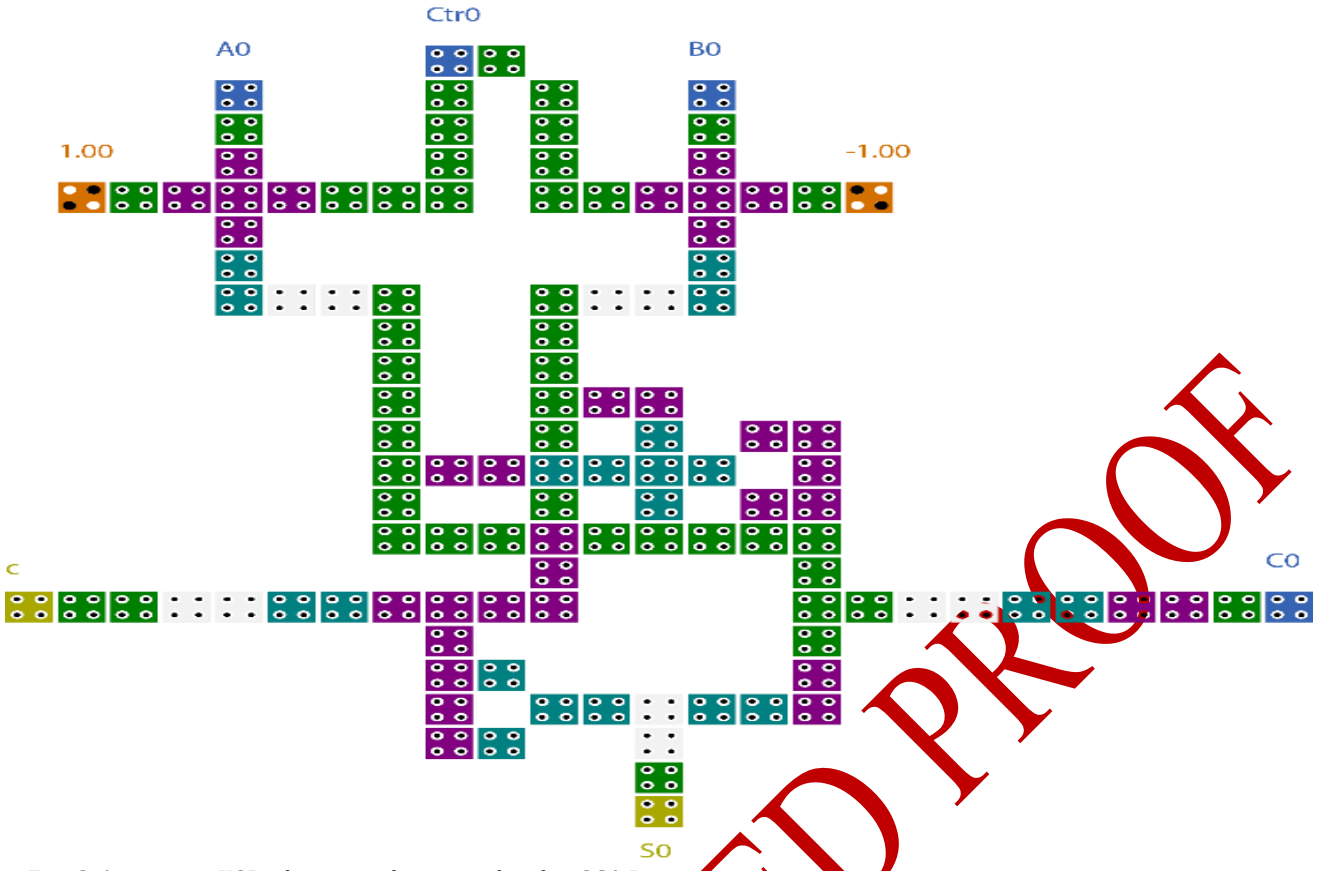

Fig. 13. Approximate XOR schematic implementation based on QCA Designer.

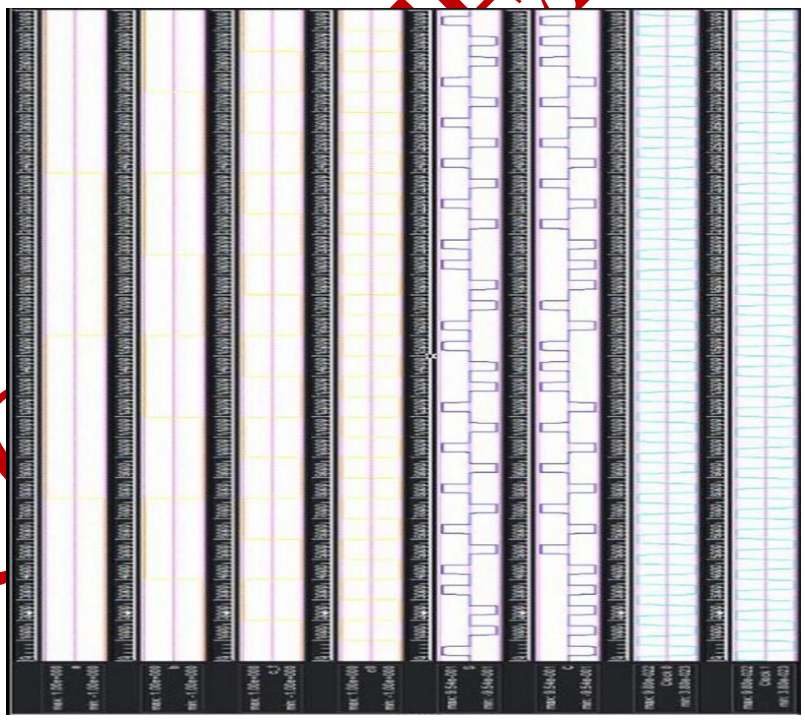

Fig. 14. QCADesigner-based XOR schematic simulation results.

Fig. 14 shows the simulation results in 4 clocks to illustrate the ratio of output to input changes. The circuit works according to the method of low-value bits in the Truncation section and high-value bits that are calculated in the exact part of the circuit, and for the exact part, two buffers are applied to the input of full-adders, which will keep the logic levels constant so that the inputs are applied with the exact source. In the approximation part, the values S0 and S1 are in the bit slicing; instead of zeroing the input values, we set them to approximate values so that the inputs in this part pass through the gate and are controlled by the C0 and C1 signals. These signals work in such a way that, for example, if C0 is given a value of zero in the OR gate,

zero is ineffective, and C will be one, which does not affect the AND gate, causing the output to receive an accurate answer. However, if the input is 1, it affects both gates. If the inputs A and B have any value, the output of the OR gate is equal to one, and the output of the AND gate is zero, and is

given to all adders. In this part, all outputs become zero regardless of input B0, so in the output, the values 1111 are added to 0000, giving the estimated value. In the full-adder part, a three-input XOR gate and a five-input MAJ function are designed, as shown in Fig. 15.

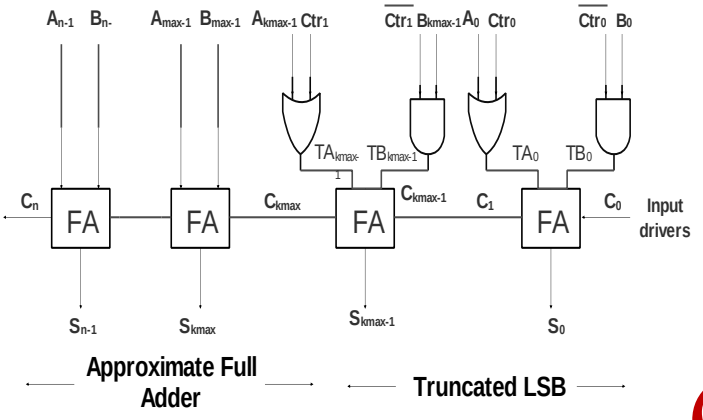

Fig. 15. The proposed bit-slicing method by the approximate full-adder.

Fig. 16. The design of a schematic approximate full-adder based on QCA Designer.

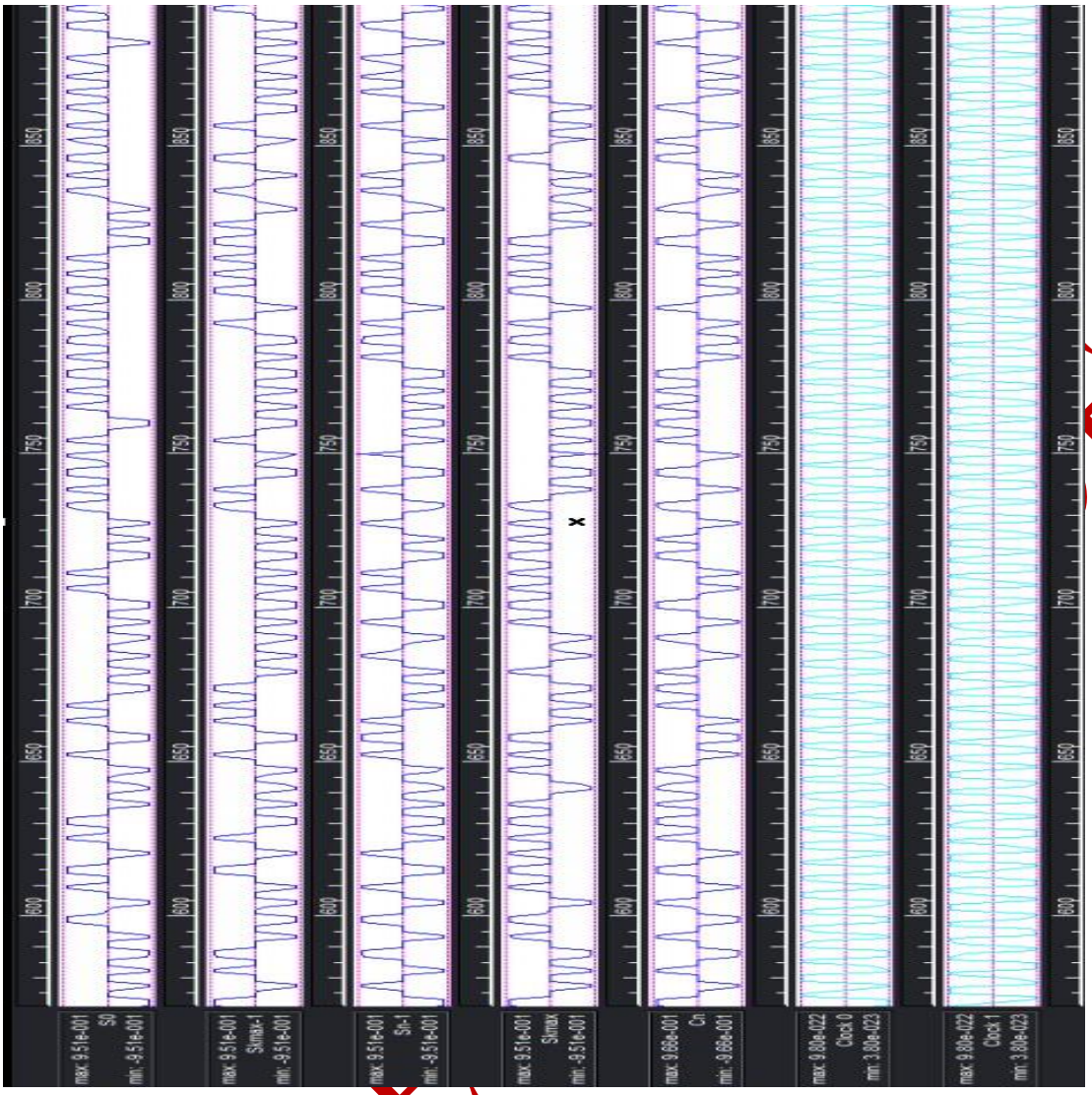

Fig. 17. The results of the approximate full-adder.

TABLE II.
The Results of the Multiplier.

A_0	B_0	A_1	B_1	P0		P1		P2	
0	0	0	0	0	✓	0	✓	0	✓
0	0	0	1	0	✓	0	✓	0	✓
0	0	1	0	0	✓	0	✓	0	✓
0	0	1	1	0	✓	0	✓	1	✓
0	1	0	0	0	✓	0	✓	0	✓
0	1	0	1	1	X	0	X	1	X
0	1	1	0	1	X	1	X	1	X
0	1	1	1	0	✓	0	✓	1	✓
1	0	0	0	0	✓	0	✓	0	✓
1	0	0	1	1	X	1	X	1	X
1	0	1	0	1	X	1	X	1	X
1	0	1	1	0	✓	1	✓	1	✓
1	1	0	0	1	✓	1	✓	0	✓
1	1	0	1	1	✓	0	✓	0	✓
1	1	1	0	1	✓	1	✓	0	✓
1	1	1	1	1	✓	0	✓	0	✓

In Table II, we check the performance of this 2 × 2 multiplier.

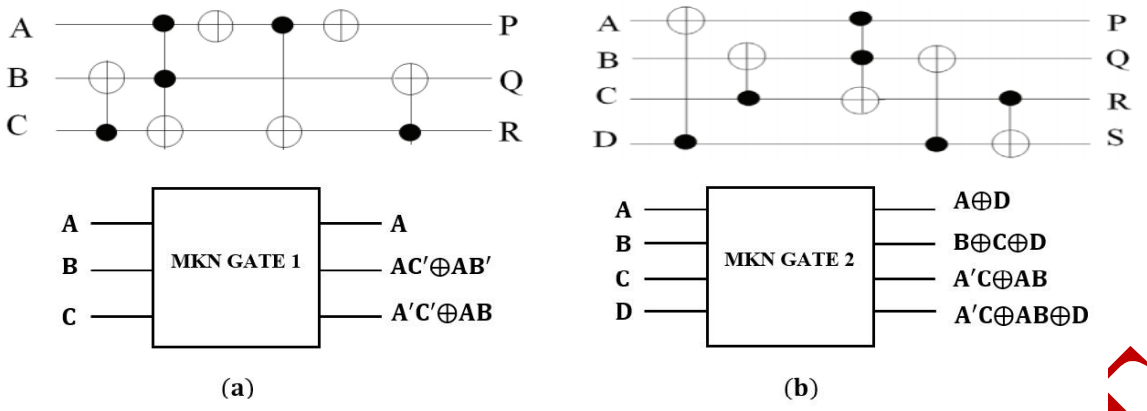

Fig. 18. The quantum structure (a) MKN1 gate, (b)MKN2 gate.

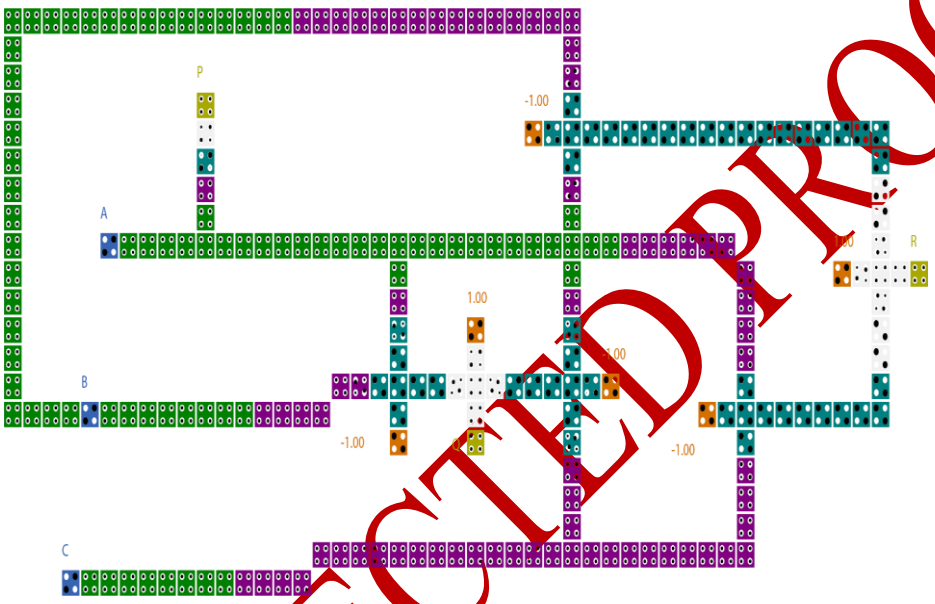

Fig. 19. MKN1 gate schematic implementation based on QCA Designer.

Fig. 20. The results of the MKN1 gate.

TABLE III

The Truth Table of the MKN1 Gate.

A	B	C	P	Q	R
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	0	0	0
1	0	0	1	1	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1

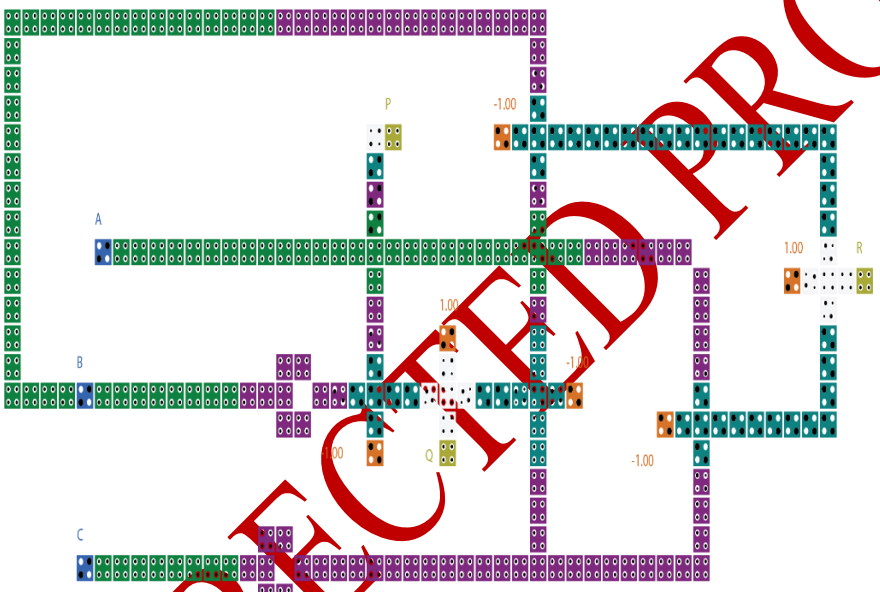

Fig. 21. MKN2 gate schematic implementation based on QCA Designer.

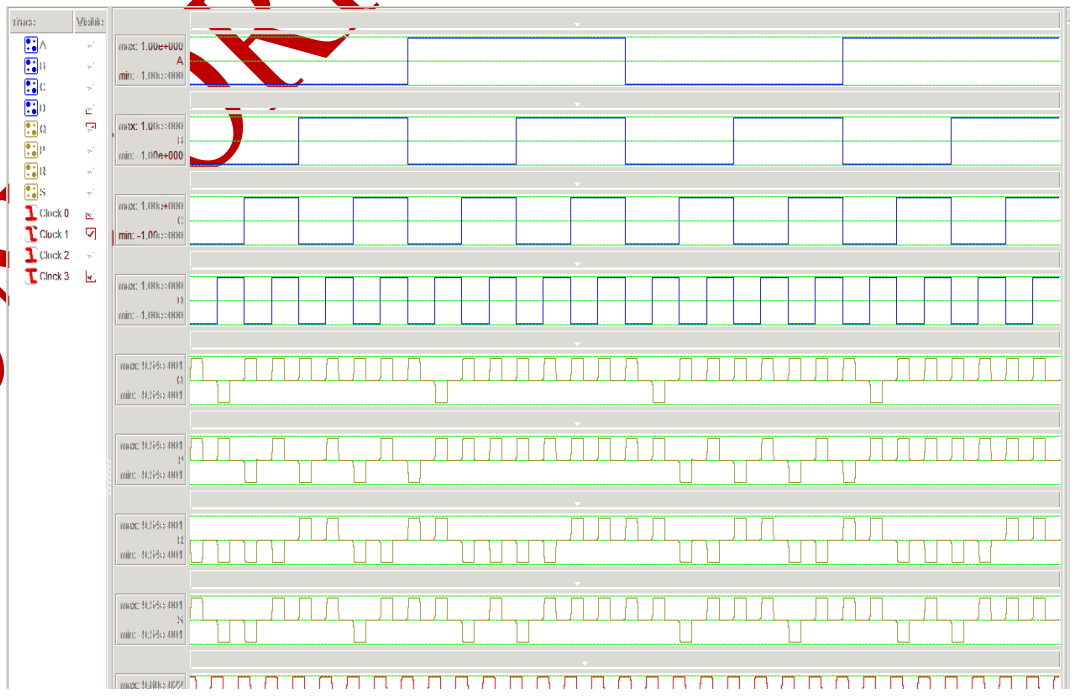

Fig. 22. The results of the MKN2 gate.

TABLE IV

The Truth Table of the MKN2 Gate.

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	1
0	0	1	0	0	1	1	1
0	0	1	1	1	1	1	1
0	1	0	0	0	1	0	0
0	1	0	1	1	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	1	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	1	1	1	1
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1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1

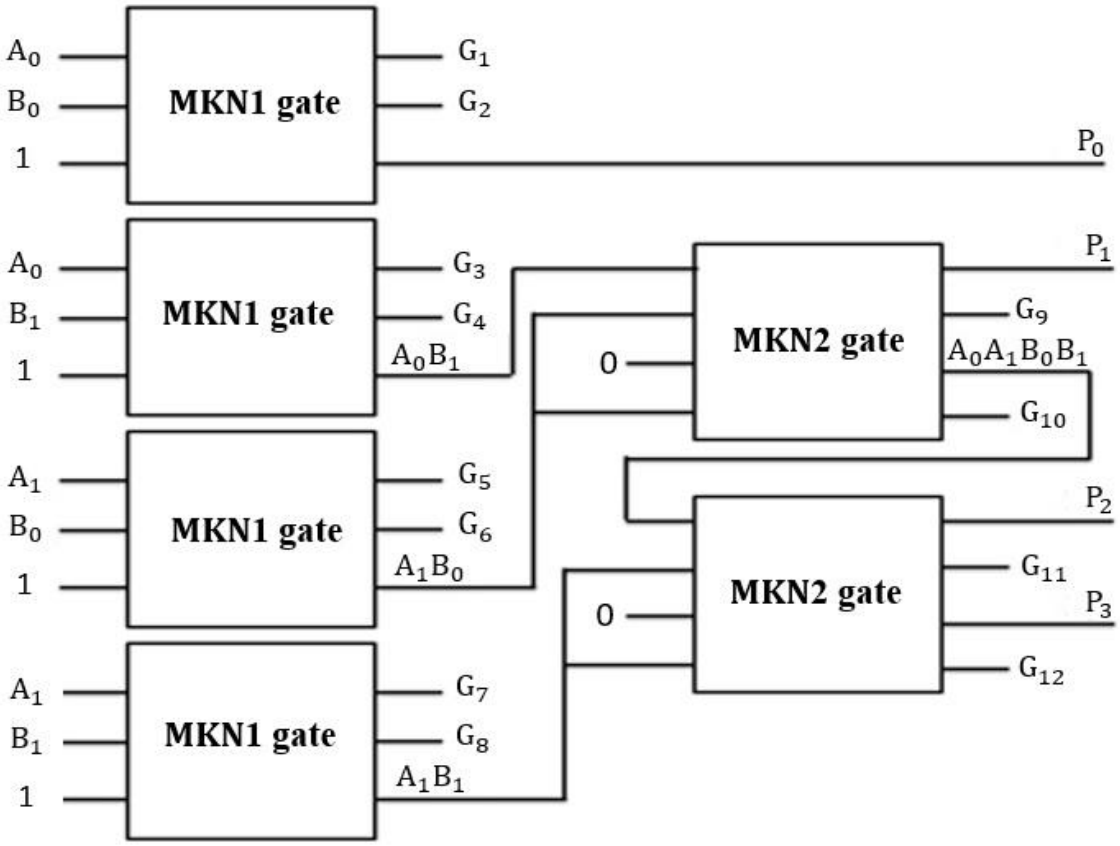

Fig. 23. The structure of a 2× 2 multiplier circuit.

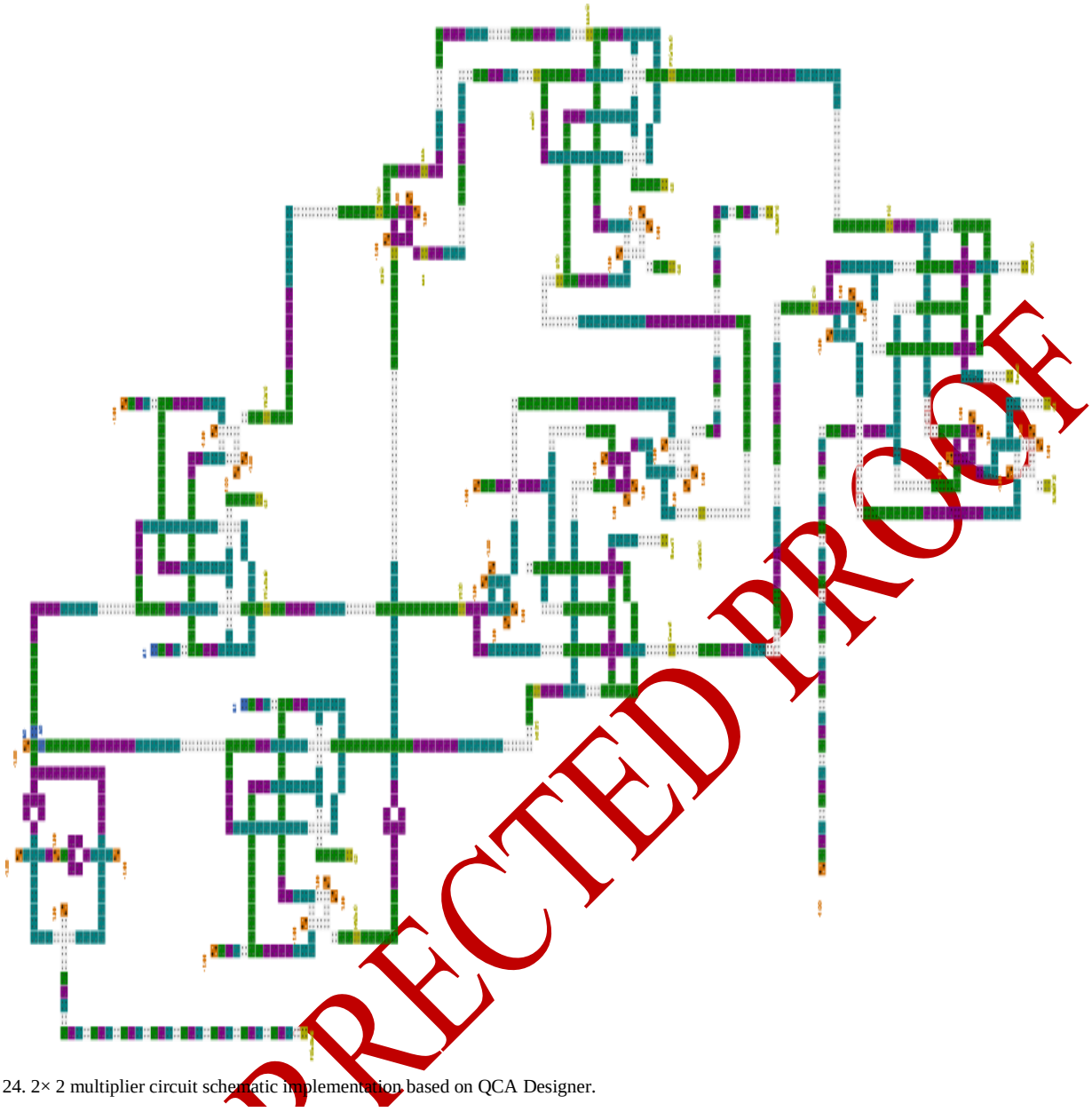

Fig. 24. 2× 2 multiplier circuit schematic implementation based on QCA Designer.

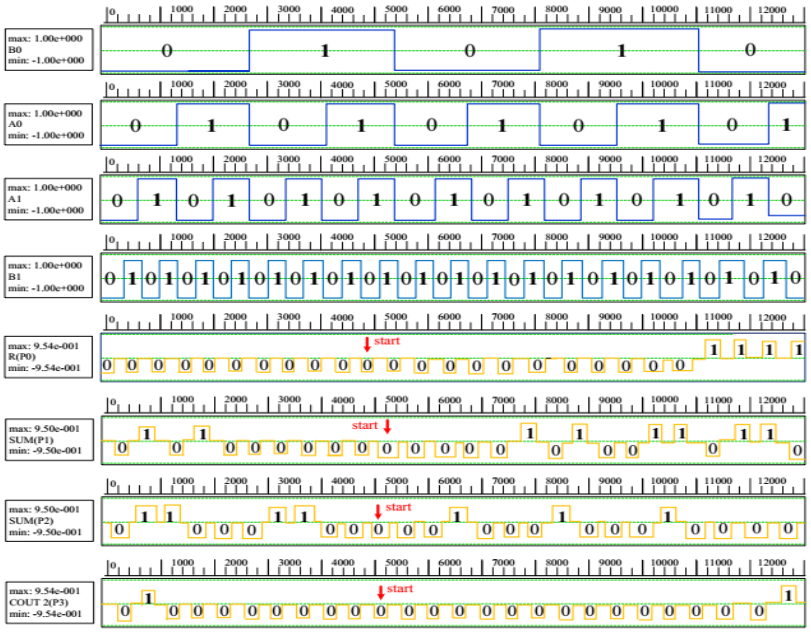

Fig. 25. The results of the 2× 2 multiplier circuit.

To rigorously evaluate the accuracy of the proposed approximate multiplier, an exhaustive error analysis is performed over all possible input combinations. For a 4-bit multiplier, this corresponds to 2^8 = 256 input cases.

For each input combination (A, B), the exact multiplication result (E_{exact}) is computed and compared with the approximate output (E_{approx}). Based on these values, the following error metrics are calculated:

Error Rate (ER):

$$ER = \frac{N_{error}}{N_{total}}$$

where N_{error} is the number of input combinations for which $E_{exact} \neq E_{approx}$, and $N_{total} = 256$.

Mean Relative Error Distance (MRED):

$$MRED = \frac{1}{256}\sum\left|\frac{E_{exact} - E_{approx}}{E_{xact}}\right|$$

Normalized Mean Error Distance (NMED):

$$NMED = \frac{1}{256}\sum\left|\frac{E_{exact} - E_{approx}}{E_{Max}}\right|$$

where E_{Max} represents the maximum possible output value, which is equal to 255 for a 4-bit multiplier.

The analysis shows that the introduced approximation primarily affects the least significant bits (LSBs). Therefore, the overall deviation from the exact result remains limited, making the proposed multiplier suitable for error-tolerant applications such as image processing and machine learning.

TABLE V

Comparison of the Performance of Existing Multipliers with the Proposed Approach.

	Proposed (circuit using MKN1 and MKN2)	**Newaz et al. [23]**	**Zhang et al. [18]**	**Zhang et al. [18]**	**Cho et al. [22]**	**Moshny et al. [20]**	**ROG Gate [21]**	**DKG Gate [19]**	**Improvement (%)**
Quantum cost	**281**	592	745	749	903	1387	993	752	79.7
Garbage output	**12**	62	43	28	49	8	5	-	80.6
Constant input	**6**	29	33	28	49	8	7	-	87.7
Number of gates	**14**	37	33	28	28	6	7	-	62.1
Area(μm2)	**0.256**	0.557	0.673	0.736	0.996	4.96	4.73	1.24	94.8
Delay(clock Zones)	**4**	6	5	5	6	7	6	5	42.8
Energy Dissipation (meV)	**0.94**	N/A	N/A	N/A	N/A	N/A	N/A	N/A	-
ER (%)	**24.22**	0	0	0	0	0	0	0	-
NMED	**0.0318**	0	0	0	0	0	0	0	-
MRED	**0.0587**	0	0	0	0	0	0	0	-

The delay values are estimated based on the critical path depth and typical QCA clocking schemes reported in the literature.

Energy dissipation for the proposed design is obtained using QCADesigner-E, whereas for existing reversible designs, energy data is not available.

Since the reference designs are exact (non-approximate) reversible multipliers, their error metrics (ER, NMED, MRED) are considered zero.

All comparisons are presented to provide both hardware and accuracy perspectives.

V. CONCLUSION

In this paper, an approximate Vedic multiplier based on QCA technology has been presented. The proposed design introduces approximation at the circuit level by modifying the full-adder units used in the partial product accumulation stage, resulting in a non-bijective (irreversible) mapping between inputs and outputs.

The multiplier is implemented using optimized QCA logic structures (MKN1 and MKN2), which reduce circuit complexity and improve layout efficiency. By combining the Urdhva Tiryakbhyam multiplication algorithm with selective approximation, the proposed architecture enables parallel partial product generation while maintaining controlled error behavior.

A comprehensive evaluation has been carried out using exhaustive simulation over all 256 input combinations. The design's accuracy has been quantified using standard error metrics, including Error Rate (ER), Normalized Mean Error Distance (NMED), and Mean Relative Error Distance (MRED), with obtained values of 24.22%, 0.0318, and 0.0587, respectively.

Performance comparison with existing reversible QCA multipliers demonstrates that the proposed design achieves significant improvements in quantum cost, area, constant inputs, and gate count. In particular, the design reduces area and circuit complexity while maintaining acceptable accuracy for approximate computing applications.

Delay is evaluated in terms of QCA clock zones, and energy dissipation is estimated using QCADesigner-E. Due to the use of majority-gate-based logic and reduced circuit depth, the proposed design is expected to exhibit improved robustness against implementation variations.

Since the reference designs are exact reversible multipliers, their error metrics are not applicable, and a fair comparison has been ensured by evaluating all designs under consistent QCA assumptions.

The proposed multiplier is particularly suitable for error-tolerant applications such as image processing and machine learning, where reduced hardware complexity and energy efficiency are prioritized over exact accuracy.

Future work will focus on detailed defect analysis, temperature-aware simulation, and application-level evaluation of power–accuracy tradeoffs.

ETHICS APPROVAL AND CONSENT TOPARTICIPATE

Not applicable.

DISCLOSURE OF POTENTIAL CONFLICTS OF INTEREST

The authors declare that they have no potential conflicts of interest.

CONSENT FOR PUBLICATION

Not applicable.

AVAILABILITY OF DATA AND MATERIALS

The data that support the findings of this study are available from the authors upon reasonable request.

COMPETING INTERESTS

The authors declare that they have no conflict of interest.

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AUTHORS' CONTRIBUTIONS

M. Bolokian: Conceptualization, Writing - original draft, Software.
Mohammad Danaie: review & editing, Software
Monireh Houshmand: Supervision - review & editing.
Hossein Boloukian: review & editing, Software

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RESEARCH INVOLVING HUMAN PARTICIPANTS AND/OR ANIMALS

Not applicable.

INFORMED CONSENT

Not applicable

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