A Novel SOI MESFET by Implanted N Layer (INL-SOI) for High Performance Applications

Hadi Shahnazarisani and Ali A. Orouji

***Abstract*— This paper introduces a novel silicon-on-insulator (SOI) metal–semiconductor field-effect transistor (MESFET) with an implanted N layer (INL-SOI MESFET) to improve the DC and radio frequency characteristics. The DC and radio frequency characteristics of the proposed structure are analyzed by the 2-D ATLAS simulator and compared with a conventional SOI MESFET (C-SOI MESFET). The simulation results show that the proposed structure has an excellent effect on the driving current. The breakdown voltage of the INL-SOI MESFET structure gets a 33.33% enhancement when compared with that of the C-SOI MESFET structure. Other main characteristics such as maximum output power density, maximum oscillation frequency, and maximum available gain have been evaluated and improved in the proposed structure.**

***Index Terms*— maximum available gain, maximum oscillation frequency, silicon on insulator (SOI), MESFET.**

I. Introduction

Silicon on insulator (SOI) technology is the most suitable offered technology for replacing the silicon bulk technology [1]. In comparison between the silicon bulk metal semiconductor field effect transistor (MESFET) and the silicon on insulator MESFET, we can understand the main difference between them, which is one layer of insulator in SOI technology. This layer creates many features in SOI devices, including high speed, low source voltage and in result low consume power. SOI MESFET is one of the new technologies and has been introduced as a low power and high performance solution with features, such as high current driving capability, low supply voltage, high current gain, and etc. Owing to the small parasitic capacitance at the source/drain, SOI MESFET technology is suitable to integrate high frequency devices. Though SOI MESFETs have excellent RF power performances, it is still worth investigation to find potential ways to improve them to better meet the increasing demand for high frequency and high power applications [2]-[3]. Over the last few years, several improved MESFET structures have been reported to achieve this goal by optimizing the device structure in order to enhance the maximum drain current or the breakdown voltage greatly [4]-[5].

The improvement of power density of the above proposed structures is very limited owing to a potential trade-off between the further increment of drain current and breakdown voltage [6]-[7]. To allow for high drain current, a large product of the channel doping and thickness ($N_C \times t_C$) is required. But, a high channel doping concentration will decrease the breakdown voltage [8]-[9]. Also, a thick channel layer will lead to a lower aspect ratio of the gate length to the channel thickness (L_G/t_C) and result in the device performance degradation [1]-[9]

In this paper, a novel SOI MESFET with an implanted N layer (INL-SOI MESFET) for improving the DC and RF characteristics is proposed. The key idea of this paper is to increase the channel doping partially by an implanted N layer (INL) in the channel region. After utilizing the INL region in the structure and optimizing its location and dimensions, the INL-SOI MESFET characteristics such as the V_{BR}, drain current (I_D), output power density, unilateral power gain (U), maximum available gain (MAG), current gain, and cut-off frequency (f_T) are analyzed and compared with a conventional SOI (C-SOI) MESFET. The results show that the INL region has an excellent effect on the device performance and can be a candidate for high-power and high-speed devices.

II. Device Structure

Fig. 1 shows the schematic cross section of INL-SOI MESFET structure. As can be seen from the figure, an implanted N layer is inserted in the channel of structure. The INL-SOI MESFET structure dimensions are as follows: The drain and source lengths are $L_D = L_S = 0.3\mu m$, gate length $L_G = 0.5\mu m$, gate–drain and gate–source spacing $L_{GD}=L_{GS}=0.5$ µm. Also, the p-type substrate layer has a thickness of 0.1 µm and the doping of 1×10^{13} cm^{-3}, the BOX region thickness is 0.4 µm, the n-type active layer is doped at 10^{17} cm^{-3} with a thickness of 0.2 µm, and the n-type cap layer doping level is 10^{20} cm^{-3}. In order to achieve the best results and due to the importance of designing a high-power device, it is important to investigate the effect of thickness, length, and doping density of the INL region on the breakdown voltage, drain saturation current, maximum output power density and maximum oscillation frequency. After optimization of the INL region dimensions, the thickness, length, and doping density of INL region are achieved 0.01 µm, 0.46 µm, and 10^{20} cm^{-3}, respectively. All the device parameters of the proposed structure are equivalent to those of the C-SOI MESFET unless otherwise stated. In order to simulate the

The authors are with the Department of Electrical Engineering, Semnan University, Semnan 35196-45399, Iran (e-mail: aliaorouji@semnan.ac.ir).

devices, ATLAS that is a 2-D simulator from Silvaco with silicon (Si) and magnificent physical models is utilized [10].

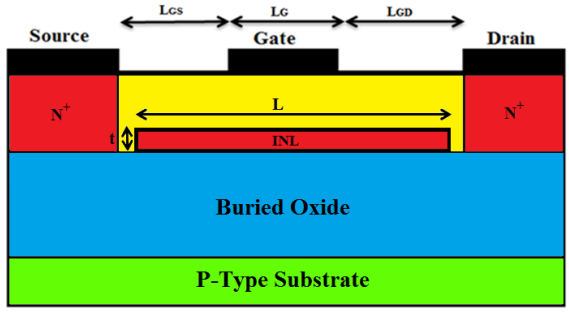


Fig. 1. Schematic cross-sectional view of INL-SOI MESFET structure.

III. DC RESULTS AND DISCUSSIONS

The negative bias of the gate goes to sending out of the electrons around the gate and putting of the holes in electron locations. Therefore, a large number of holes surround the gate. The Gauss law is given by [11]:

$$\frac{\partial E}{\partial x} = \frac{\rho}{\varepsilon s} = \frac{q(p-n+N_D-N_A)}{\varepsilon_S} \quad (1)$$

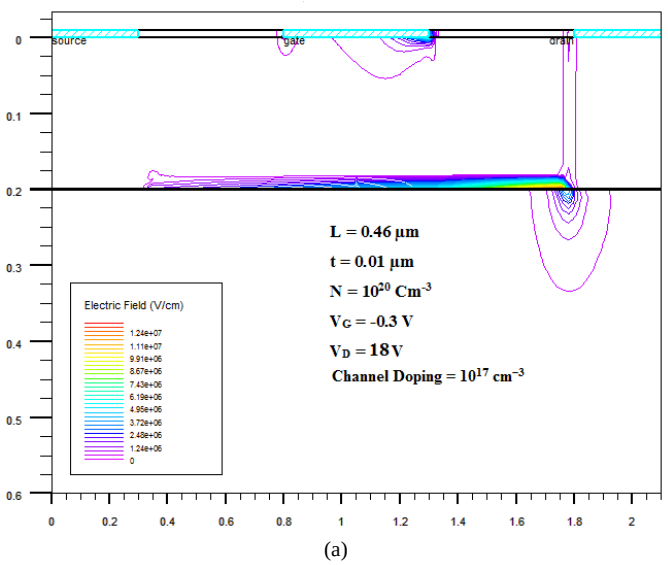
where, E is the electric field, ε_S the semiconductor permittivity, ρ is the charge density, p is the hole concentration, n is the electron concentration, N_A is the acceptor concentration, and N_D is the donor concentration. According to Fig. 2 (a) and (b), the lower hole concentration around the gate of the INL-SOI MESFET structure reduces the electric field crowding of the device, and the lower electric field crowding around the gate leads to an increase of the V_{BR}. It decreases the electric field crowding near the gate edge, modifies the electric field in the channel, and modulates the surface electric field distribution. Thus, a higher voltage is required for the electric field of the INL-SOI MESFET structure to reach the critical amount.

Simulation results in Fig. 3 illustrate that the INL-SOI MESFET structure increases the breakdown voltage (V_{BR}) and drain current (I_D) at V_{DS}=17 V and V_{GS} = -0.3 V. According to the figure, the breakdown voltage (V_{BR}) of the INL-SOI MESFET structure is about 33.33% larger than that of the C-SOI MESFET structure and drain current (I_D) of the INL-SOI MESFET structure is about 166.66% larger than that of the C-SOI MESFET structure. To allow for high drain current, a large product of the channel doping and thickness (N × a) is required [12].

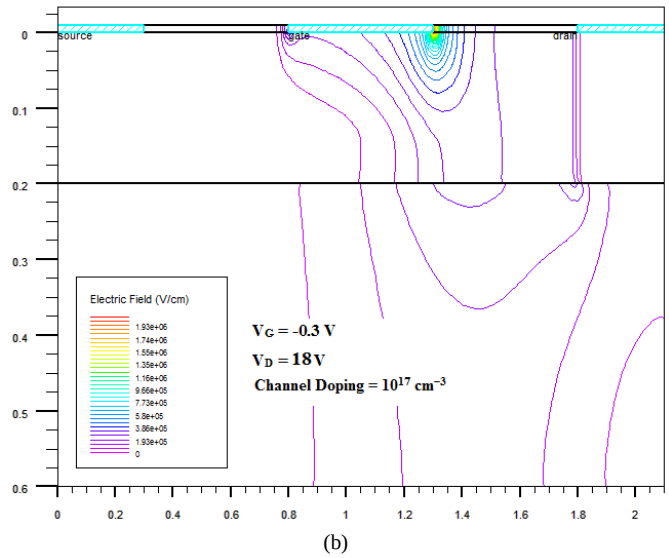
Fig. 4 (a) and (b) show the out of the ordinary effect of the INL region in distributing the potential lines toward the drain. This means that, by utilizing the INL region in the suggested structure, the equipotential contours are evenly spaced in comparison with that of the C-SOI MESFET structure. In the C-SOI MESFET structure, the potential is crowded at the gate edge, which leads to the gathering of high electric field in the Si surface under the gate edge, but in the INL-SOIMESFET structure, the potential crowding at the gate edge is weakened due to the effect of INL region. The theoretical maximum output power density (P_{max}) is given as follows [12]:

$$P_{max} = \frac{I_{Dsat}(V_{BR}-V_{Knee})}{8} \quad (2)$$

where, I_{Dsat} is the drain saturation current and V_{Knee} is the knee voltage and V_{BR} is the breakdown voltage.



(a)



(b)

Fig. 2. Two-dimensional distribution of the electric field lines for the (a) INL-SOI MESFET and (b) C-SOI MESFET.

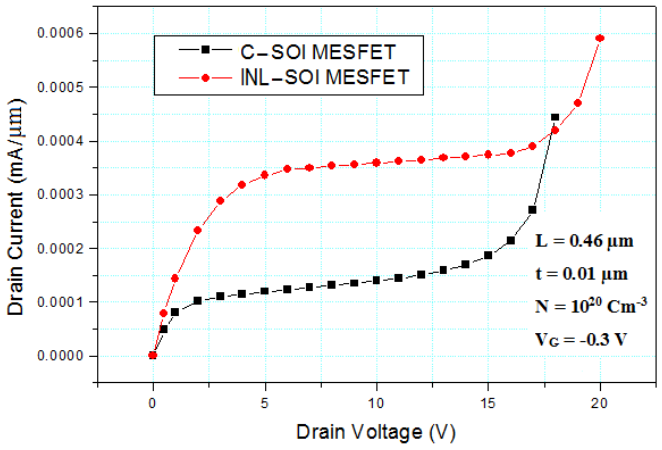
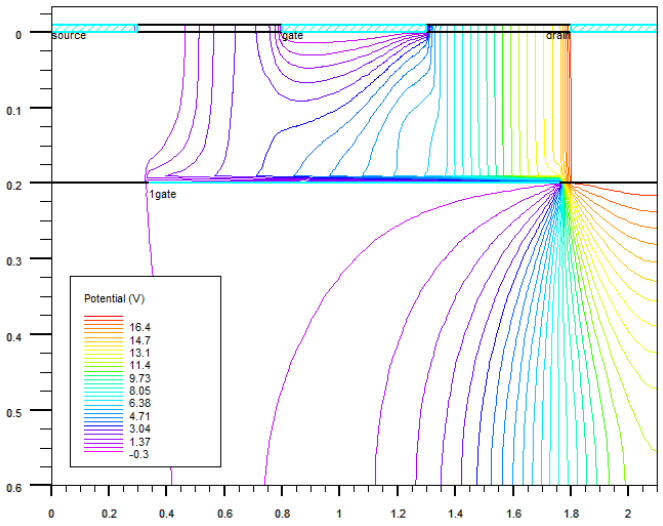
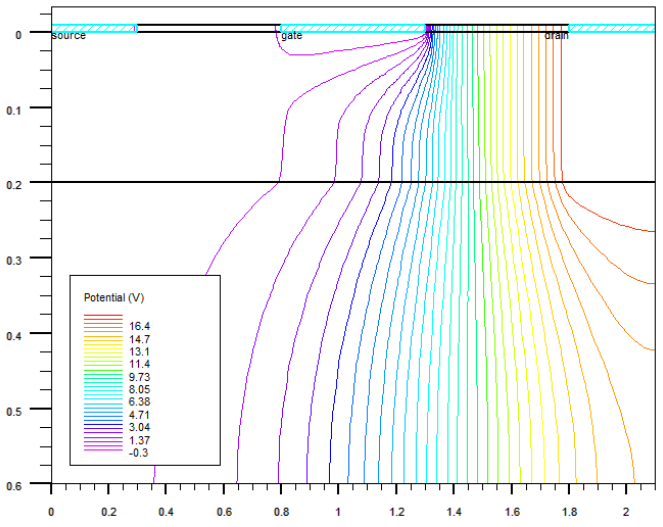


Fig. 3. Breakdown voltage (V_{BR}) and drain current (I_D) as a function of the gate-source voltage and drain-source voltage for both the structures at V_{GS}=-0.3 V.



(a)



(b)

Fig. 4. The out of the ordinary effect of the implanted N layer in distributing the potential lines toward the drain for the (a) INL-SOIMESFET and (b) C-SOI MESFET.

Therefore, the maximum output power densities (P_{max}) are 0.550 and 0.168 W/mm for the INL-SOIMESFET and C-SOI MESFET, respectively. Thus, a 227.38% enhancement in the P_{max} of the proposed structure is achieved.

IV. RF Results And Discussions

This section describes the RF characteristics of the proposed structure. Unilateral power gain, trans-conductance, maximum available gain and current gain versus the frequency have been illustrated in Fig. 5 to 8 for V_{DS}=10 V and V_{GS}=-0.3V conditions. The frequency range starts from 1 GHz to 3 GHz. As can be seen from these figures, the mentioned gains improve due to the INL region.

Figs. 9 and 10 show the gate-source capacitance and the drain conductance as a function of frequency for both the structures at V_{DS}=10V and V_{GS}=-0.3V conditions, respectively. As can be seen from these figures, the proposed structure has smaller the gate-source capacitance and the drain conductance in comparison with the C-SOI MESFET structure.

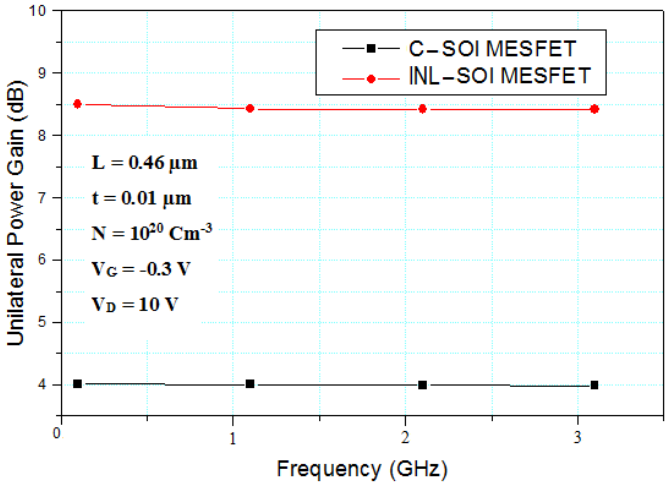


Fig. 5. Unilateral power gain versus frequency for both the structures.

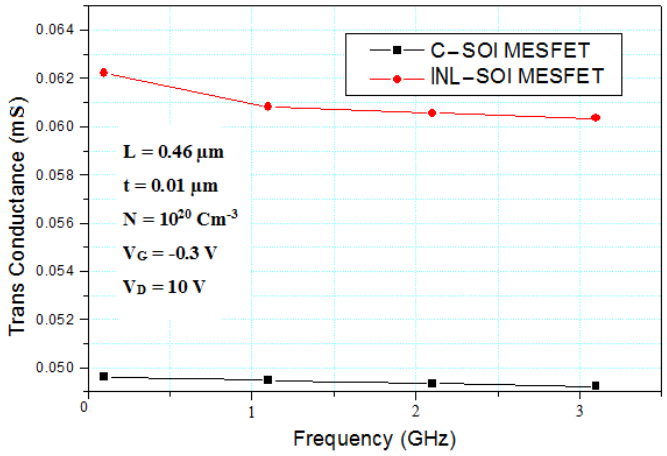


Fig. 6. Trans-conductance as a function of frequency for both the structures.

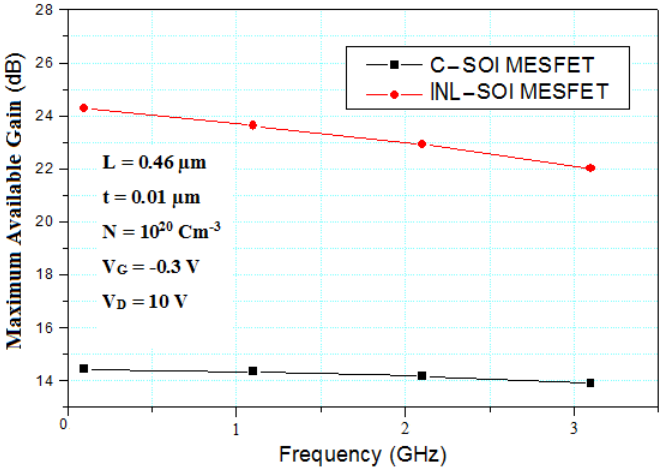


Fig. 7. Maximum transducer available gain versus frequency for the INL-SOI and C-SOI MESFET structures.

Two important high frequency parameters fora transistor are cut-off frequency (f_T) and maximum oscillation frequency (f_{max}).These parameters can be calculated from the following equations [13]. g_m is the maximum DC trans-conductance and c_{gs} is the gate-source capacitance [11]-[14].

$$f_T = \frac{g_m}{2\pi C_{gs}} \quad (3)$$

$$f_{max} = \frac{f_T}{2}\sqrt{\frac{R_{ds}}{R_g}} \quad (4)$$

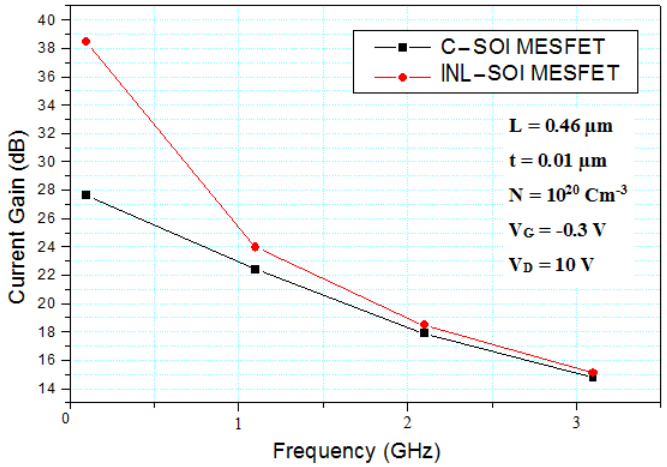


Fig. 8. Comparison of the Current gain for the INL-SOI and C-SOI MESFET structures.

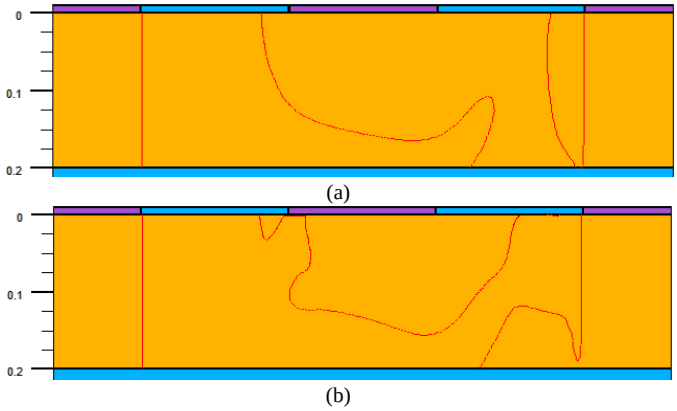


Fig. 9. Two-dimensional distribution of the depletion region for the (a) INL-SOI and (b) C-SOI.

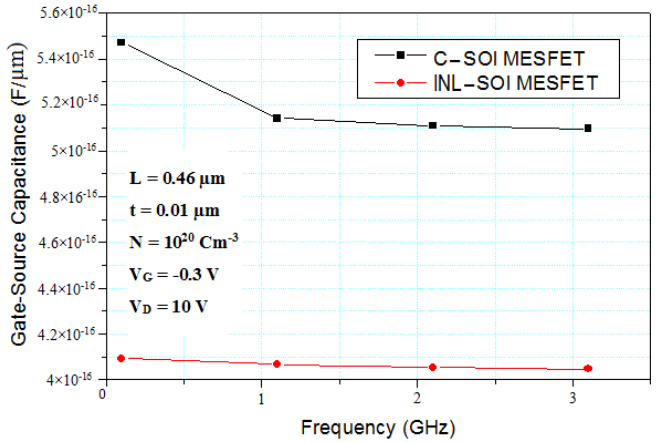


Fig. 10. Gate-source capacitance versus frequency for both the structures.

The two above equations show that a larger g_m/c_{gs} ratio, augments the f_T and f_{max}. The results illustrated in Figs. 6 and 11 show that the proposed structure has larger g_m and smaller c_{gs} in comparison with the conventional structure.

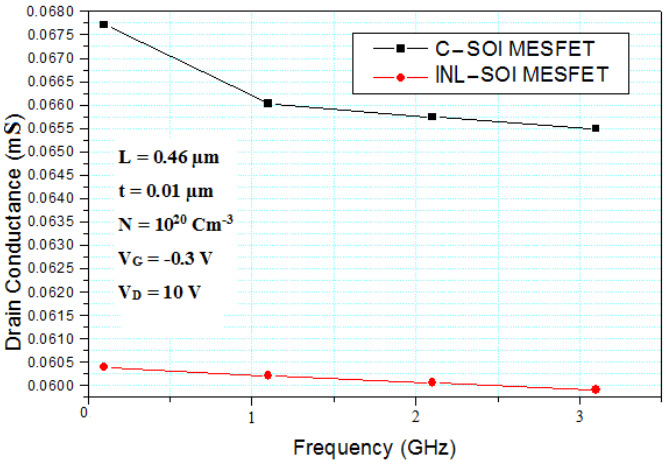


Fig. 11. Comparison of the drain conductance for the INL-SOI and C-SOI MESFET structures.

The capacitance equation can be expressed as follows:

$$C = \varepsilon_S A/d \quad (5)$$

Where, ε_S is the semiconductor permittivity, A is the area of the capacitance plates, and d is the distance between capacitance plates. In semiconductor devices, d is considered as the distance between metals and the depletion region around them. As can be seen in Fig. 9, which comparison of the depletion region as around the gate edge for two structures. According to Fig. 9 the depletion region around the gate edge in the proposed structure is more than the conventional structure then the gate-source or gate-drain capacitance in the INL-SOI is less than the C-SOI.

V. Optimization And Dimensions

In order to achieve the best results and because of the importance of designing a high-power device, it is important to optimize the INL parameters carefully. At first, the INL with

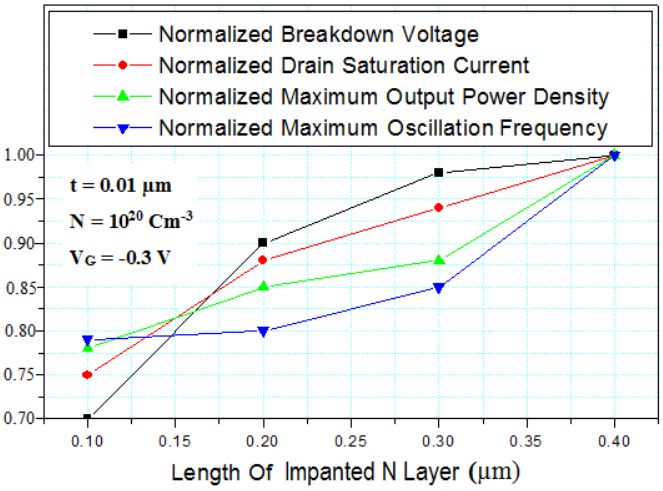


Fig. 12. Comparison of normalized parameters according to length of INL region.

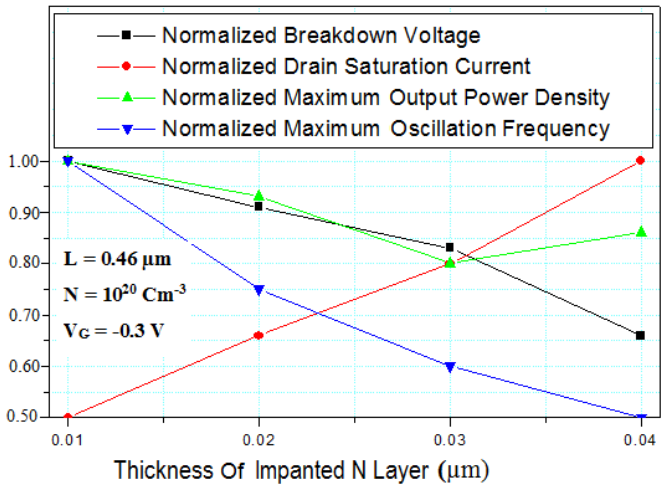


Fig. 13. Comparison of normalized parameters according to thickness of INL.

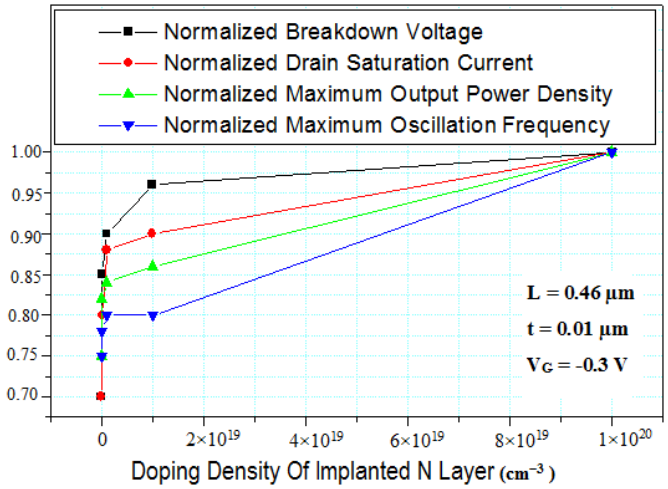


Fig. 14. Comparison of normalized parameters according to doping density of INL region.

specific dimensions is considered in the channel region, and by changing its location, the best place for situating it, is achieved; after determining the INL best situation, it is important to appoint the thickness, length, and doping density of INL region. The initial values of L, t, and N are determined as 0.46 µm, 0.01µm, and 10^{20} cm^{-3}, respectively.

In order to achieve the best results and the importance of designing a high-power device, it is important to investigate the effect of thickness, length, and doping density of the INL region on the breakdown voltage, drain saturation current, maximum output power density and maximum oscillation frequency.

By increasing the length and decreasing the thickness of INL region, more repetitive electric field and higher V_{BR} are expected to be achieved. As the breakdown occurs near the gate edge beside the drain, so when the INL length increases, the V_{BR}, drain saturation current, maximum output power density, and maximum oscillation frequency improve. Also, when the INL thickness decreases the breakdown voltage, maximum output power density, and maximum oscillation frequency increase but the drain saturation current reduces. These results show in Figs. 12 and 13.

The doping density of INL region affects significantly the device characteristics. By increasing the doping density of INL,
the breakdown voltage, drain saturation current, maximum output power density, and maximum oscillation frequency of the INL-SOI MESFET increase as can be seen from Fig. 14.

VI. Conclusion

DC and RF characteristics of a novel SOI MESFET with an implanted N layer (INL) have been analyzed by 2-D numerical simulations. Gate distribution lowers electric field crowding around the gate and improves breakdown voltage (V_{BR}). The V_{BR} of the INL-SOI MESFET structure is enhanced significantly by 33.33% compared with that of the C-SOI MESFET structure and drain current (I_D) of the INL-SOI MESFET structure is enhanced significantly by 166.66% compared with that of the C-SOI MESFET structure. The maximum output power density of the INL-SOI MESFET structure increases meaningfully by 227.38% compared with that of the C-SOI MESFET structure. The maximum oscillation frequency and MAG of the proposed structure excellent improve in INL-SOI MESFET structure with those of the C-SOI MESFET structure. Unilateral power gain, trans-conductance, maximum transducer power gain, and current gain have been improved in the INL-SOI MESFET structure compared with that of the C-SOI MESFET structure. Therefore, the proposed structure has greater electrical performances than the C-SOI MESFET structure and it can be taken into consideration for high-power and high-speed applications.

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