Expanded Channel in the SOI MESFET by SiGe Regions to Improve the Current Capability and High-Frequency Features

Behrooz Fath-Gangi[1], Ali Mir[1]*, Ali Naderi[2], Reza Talebzadeh[3], Ali Farmani [3]

Abstract **— In this paper, a novel structure for silicon on insulator metal semiconductor field effect transistors (SOI MESFETs) is introduced using the heterogeneous Si/SiGe region. SiGe semiconductor is used to expand the effective width of the drift region inside the buried oxide (BOX) layer. Due to its properties such as high electron mobility, high electron drift velocity, and excellent radio frequency (RF) performance, it significantly increases the current density of drain and other DC and RF parameters. Also, to control the critical electric field, which determines the breakdown voltage of the device, as well as to reduce the parasitic capacitance to improve its frequency characteristics, an additional oxide region between the gate and drain and below a part of the gate region is used. Numerical simulation shows that the drain current density and breakdown voltage of the proposed device compared to the conventional structure has been improved by 120% and 37%, respectively, resulting in a 2 times increase in maximum output power density (P_{max}). Also, the RF specifications of the new structure, including current gain (h_{21}), unilateral power gain (U), and maximum available power gain (MAG), have been improved by 130%, 85%, and 65%, respectively. These specifications are proper for a device in high power and RF circuits like D-band applications.**

Index Terms **—** Breakdown voltage, Current density, Electric field, Frequency characteristics, Maximum output power density, SOI MESFET.

I. INTRODUCTION

Insulating silicon technology, briefly called SOI, uses a layer of silicon on an insulating layer to make electronic devices. In recent years, this technology has attracted the attention of researchers and has led to desirable advances in the design of electronic devices [1-4]. The SOI MESFET is a device that consists of three parts: a channel, a buried oxide (BOX), and a substrate [5,6]. SOI technology has higher reliability and efficiency rather than body silicon technology. In body silicon technology, there are parasitic capacitance effects and leakage current originating from the silicon substrate [7], but in SOI technology, it has been eliminated due to the use of proper insulation. For this reason, parasitic capacitances are reduced effectively, so it will be possible to work at high frequencies more easily [8]. The speed of the devices based on the mentioned technology is very high [9]. The dominant technology in integrated circuits is based on the design of MOSFET and CMOS devices [10]. There are some problems for transistors in this technology such as leakage current and radiative sensitivity under the gate, the strong dependence on the device parameters, and the large device size that have led the researchers to seek to eliminate these defects or replace them with a new structure with better performance [11]. SOI MESFET transistor takes advantage of both SOI technology and MESFET [12]. Some of SOI MESFET specifications are low leakage current and proper isolation [13], less noise, more electron mobility, and consequently higher speed-reduced parasitic capacitances, and as a result more desirable frequency characteristics [14], fluctuations below the threshold [15], low power consumption and small size due to the lack of substrate oxide, greater scalability, and insensitivity to radiation [16]. So, it can be used in integrated circuits and also as an isolated device in specified applications. Despite such desirable advantages, in this structure, the breakdown voltage and output current are slightly low. The relationship between breakdown voltage and the drain current is in the form of the swap, in a way increasing one of them causes the other to decrease, and vice versa, so increasing the P_{max} is restricted. It is noteworthy that increasing the impurity and channel width increases the current in the drain and reduces the breakdown voltage [17-22]. The breakdown voltage in SOI MESFET mostly occurs because of ionization after the collision. The high gradient potential

1. Electronic Engineering, Faculty of Engineering, Lorestan University, Khoram-Abad, Iran.
2.Faculty of Engineering, Imam Khomeini International University, Ghazvin, Iran.
3. Faculty of Engineering, Lorestan University, Khoram-Abad, Lorestan, Iran.
Corresponding author: mir.a@lu.ac.ir

lines at the gate edge next to the drain produce a strong field, which causes high-impact ionization and breakdown at the gate corner [23]. Low breakdown voltage inhibits the transistor's ability to operate in high-current, high-power applications, which lowers the device's power density [24].

Therefore, in recent years, extensive research has been done by researchers on SOI MESFETs to develop the performance of this equipment. Since the effect of increasing the field and causing breakdown at the edge of the gate is more likely, various research, have attempted to control the electric field in this zone. In literature, silicon oxide has been used in this zone, because it has a larger critical field than Si [25]. Also, the nickel used inside the channel or the buried oxide region causes the potential line to spread inside the channel and reduce the electric field around the gate [26]. Furthermore, the electric field can be controlled with a combination of the two methods mentioned before [27]. In some studies, creating high and low resistance boxes in the carrier's way and the change of channel impurities have improved the breakdown of the suggested structure beside the drift current [28].

Si/SiGe structures have been used in different applications, including bipolar and optoelectronic devices [29]. By means of Si and SiGe alloys, high-quality heterogeneous connections can be created. In our new structure, using the heterogeneous structure of Si/SiGe is introduced. The semiconductor $Si_{1-x}Ge_x$ is used to expand the channel inside a part of the buried oxide layer, where the molar fraction x = 0.2 is assumed to be the default. The electron mobility of SiGe in doping with $1.5 \times 10^{17} cm^{-3}$ n-type impurity and at room temperature is about 30% more than Si [30]. SiGe semiconductor is used to expand the effective width of the drift region inside the buried oxide (BOX) layer. The power density and drain current both dramatically rise along with the acceleration of electron motion. An oxide box between the gate and drain and below a portion of the gate, is also used to control the electric field at the corner of the gate close to the drain, which results in a breakdown in the device. These adjustments have concurrently increased the device's breakdown voltage and drain current, two key features; as a result, the output power has also improved in the new structure. Also, the RF characteristics of the new structure have improved. The devices are simulated by two-dimensional (2D) numerical simulator Silvaco, Atlas module [31]. The paper is organized as follows. In section II, the schematic view of the proposed structure, the parameters required to simulate, and the process of fabricating the new structure are presented. Sections III and IV show the results of DC and RF simulations. Finally, the discussion, optimization, and conclusions are included in sections V and VI respectively.

II. DEVICE STRUCTURE AND SIMULATION METHOD

The schematic of the suggested structure is shown in Fig.1. In comparison with the basic structure, it uses a heterogeneous Si/SiGe structure. SiGe semiconductor is used to develop the channel inside a part of the BOX layer. Due to its properties such as high mobility of carriers, high speed, and excellent frequency performance, it is expected to improve the current in the drain, the current gain, and other related DC and RF parameters. To control the critical electric field that leads to the breakdown voltage, use an oxide box between the gate and drain and below a part of the gate. The oxide material is SiO_2. The dimensions of the oxide zone added between the gate and the drain, and the SiGe region added inside the buried oxide are optimized according to the desired results after several simulations.

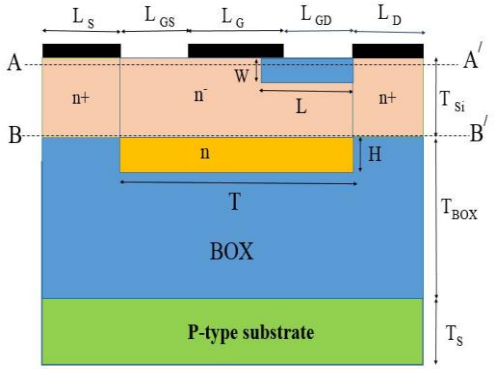


Fig.1. Schematic view of the proposed structure.

The essential parameters containing the size and amount of impurities of the areas, to simulate the proposed structure are given in Table I. It should be noted that for accurate comparison between two structures, all common parameters between the two structures are considered to be equal.

TABLE I
Utilized Parameters for Simulation of the Devices.

Parameter	Symbol	Value
Length of source/drain	L_S / L_G	0.3 µm
Gate length	L_G	0.5 µm
Space between the gate and source/drain	L_{GS} / L_{GD}	0.5 µm
Length of oxide part	L	0.75 µm
Height of oxide part	W	0.06 µm
Length of SiGe part	T	1.5 µm
Height of SiGe part	H	0.07 µm
The silicon thickness	T_{si}	0.2 µm
The BOX region thickness	T_{BOX}	0.4 µm
The substrate thickness	T_s	0.1 µm
Doping of channel	n^-	$10^{17} cm^{-3}$
Doping of SiGe part	n	$1.5\times10^{17} cm^{-3}$
Doping of Source/drain	n^+	$1.0\times10^{20} cm^{-3}$
Doping of Substrate	p^{--}	$1.0\times10^{13} cm^{-3}$
Gate work-function	ϕ	5.1 eV

The values of the *L*, *W*, *T*, and *H* parameters given in the table are optimized, which are described in the following sections.

The sample process of fabricating the new proposed structure is depicted in Fig. 2. We need two silicon wafers A and B to develop the proposed device. Wafer A with an an impurity of p-type has the direction of ‹100› and wafer B with an impurity of n-type has the direction of ‹100› (Fig. 2 (a)). On wafer A, an oxide is deposited as a substrate, which is called buried oxide (Fig. 2 (b)). In the next step, in order to create a SiGe region on a part of the oxide, via definition is done (Fig. 2 (c)) and the SiGe layer is created on the oxide with n-type impurity. (Fig. 2 (d)). In the next step, using the chemical mechanical planarization (CMP) method, the extra parts of SiGe in the previous stage of fabrication are removed and its surface is smoothed and polished (Fig. 2 (e)). Now the wafer B, which is considered as the channel and the active part of the structure, is bonded to the previous part (Fig.2 (f)). For wafer B, via definition is done to create the oxide between the gate and drain (Fig. 2 (g)). Now, on the surface of the structure, the oxide is deposited and the previously created area is filled with oxide (Fig. 2 (h)). In this step, the excess oxide parts of the previous step are removed by the CMP method and its surface is completely smooth and clean (Fig. 2(i)). The final stage of fabrication involves determining the doping and location of the electrodes in the drain, source, and gate areas (Fig. 2 (j)). For fabricating of new device, the conventional steps are used. It should be mentioned that a different method of fabricating SOI MESFET called Smart Cut [32], may be used to fabricate the proposed device.

The results of the research are simulated by a 2D numerical simulator Silvaco Atlas module and the consequences are compared with the results of the basic device. The Atlas module is based on mathematical and numerical models, which describe the physical phenomena in semiconductor devices. The Poisson equation, which analyses the spatial fluctuations of potential and electric field in semiconductors, and the continuity equation, which looks at the variations in carrier density over time in semiconductors, are among the fundamental equations of semiconductors [2]. To confirm the correct operation of the two-dimensional ATLAS simulator and the accuracy of its results, the simulator must be calibrated with experimental data [1]. Fig. 3 illustrates the characteristics of the current and voltage of the drain at different bias voltages of the gate, for experimental data and simulated results. It is visible that simulation results and experimental data are fairly matched. To match the simulation results with experimental data and these results are closer to reality, different physical models should be activated, which are: Fldmob, SRH, BBT-STD, impact Selb, incomplete, Auger, and Analytic models [31].

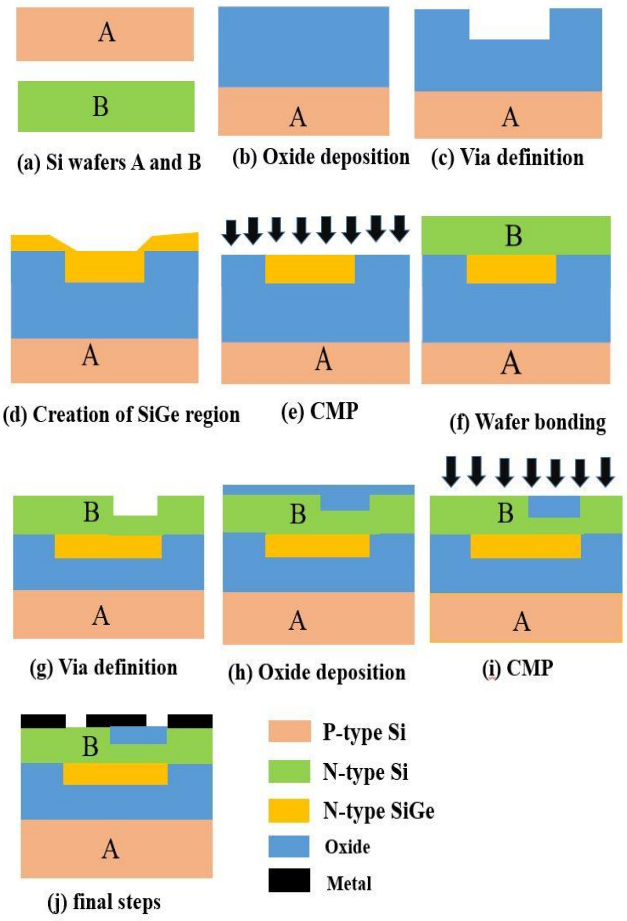


Fig. 2. (a to j) The sample process steps for fabricating the proposed structure.

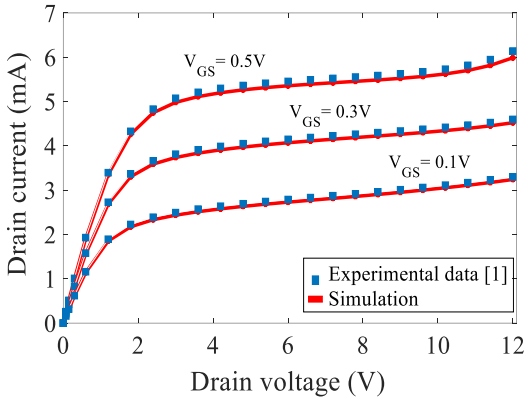
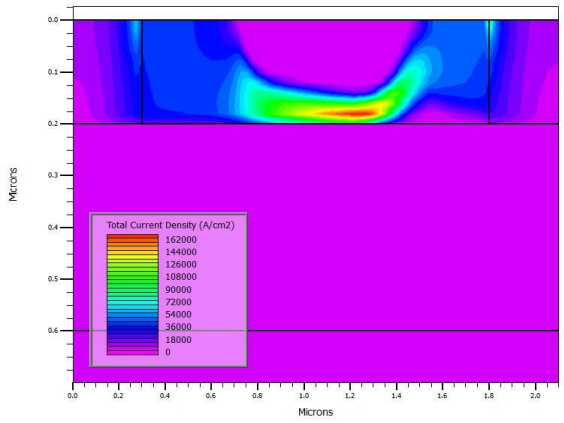


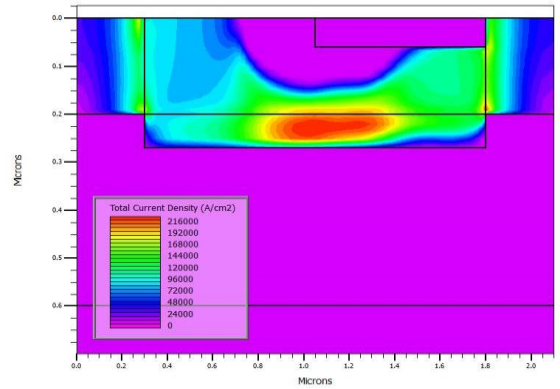
Fig. 3. Comparison of simulated structure results with experimental data [1].

III. DC SIMULATION RESULTS

Fig. 4 shows the 2D distribution of current density and Fig. 5 shows the total current density along the BB′ cutline in the basic structure and its proposed counterpart



(a)



(b)

Fig.4. Two-dimensional distribution of current density, conventional structure (a), and Proposed structure (b) at V_{GS} = - 0.5V and V_{DS} = 5 V.

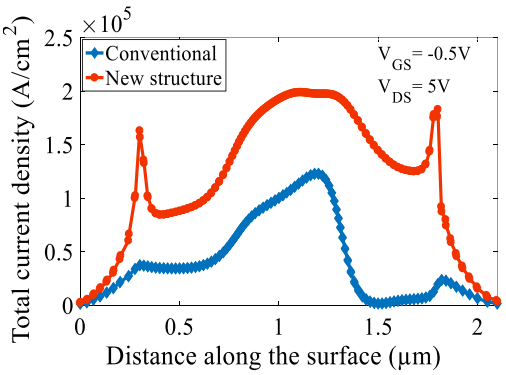


Fig.5. Total current density in the basic and the proposed structures for V_{GS} = -0.5V and V_{DS} = 5 V along BB′ cutline

for V_{GS} = - 0.5V and V_{DS} = 5V. By creating a SiGe n-type region with 1.5×10^{17} cm^{-3} impurity to reduce the channel resistance inside a part of the BOX, the effective channel width increases, and also, because of the high electron mobility of SiGe semiconductor, the current density will improve. Furthermore, due to the existence of the oxide box between the gate and the drain, which causes the potential lines to be scattered inside the channel, the needed applied voltage to the channel is reduced. As a result, it reduces the width of the depletion region. In other words, the oxide region acts as a useful separator and prevents the depletion region below the gate from spreading to the channel zone. For the mentioned reasons, the effective width of the channel for the passage of carriers has increased, which leads to enhancing the current density of the proposed device.

In Fig. 6, the characteristics curve of the drain current is displayed for V_{GS} = -0.5V and V_{GS} = 0.5V for basic and proposed structures. The drift current in a SOI MESFET depends effectively on the effective channel width, charge density, electron mobility, and channel electric field. It is described by the following relation [12]:

$$I_D = Z[h - h(x)] \times eN_d \times \mu_n \times \frac{dv}{dx} \qquad (1)$$

where *h* is the channel thickness, e is the electron charge, N_d is the concentration of the donor dopant, and *h(x)* is the discharge region width. Consequently, *h-h (x)* is the effective channel width. The excess SiGe region inside the buried oxide increases *h*. The oxide region between the gate-drain reduces the voltage *V(x)*. Thus *h(x)* decreases according to the following equation [26].

$$h(x) = \left(\frac{2\varepsilon(\psi_{bi} + V(x) - V_G)}{eN_d}\right)^{1/2} \qquad (2)$$

where V(x) is the voltage of the channel and Ψ_{bi} is the build-in voltage. As a result, in Eq. (1), increasing *h-h(x)* raises the drain current. Another effective factor is the use of SiGe semiconductor with high electron mobility (μ_n) inside the channel, which according to Eq. (1) increases the drain current. According to the mentioned reasons and from Fig. (6), the drain current in the proposed structure shows a significant growth equal to 120% compared to the basic structure. This growth in current will improve the P_{max} of the new structure compared to the conventional structure, which we will discuss in the following.

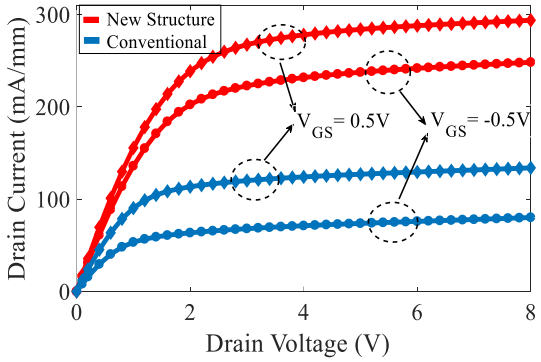


Fig. 6. Output characteristics of the basic and the proposed structure, for V_{GS} = 0.5V and -0.5V.

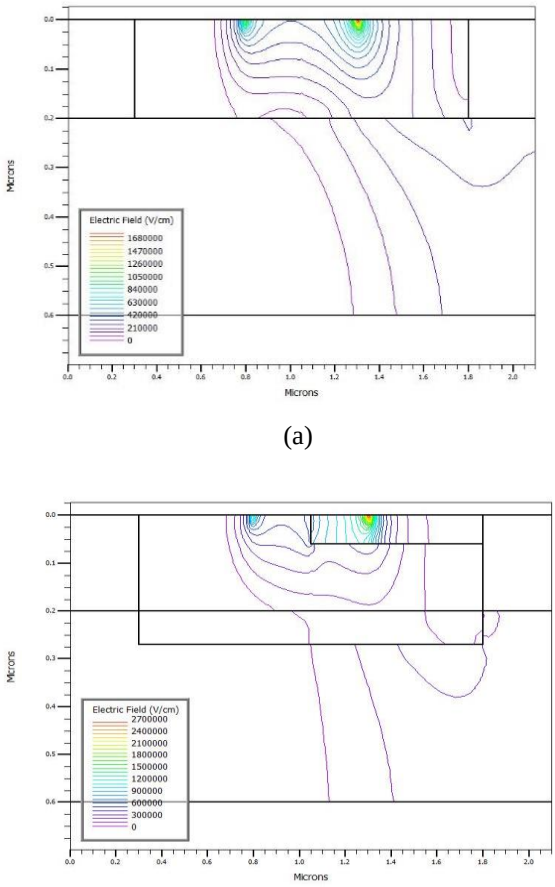
Where the electric field is strong and reaches a critical level, a breakdown happens. It mainly happens at the edge of the gate near the drain of SOI MESFET transistors, which has a strong electric field. When the kinetic energy of the carriers rises above the energy gap in strong electric fields, impact ionization produces a pair of holes and electrons. Repetition of this procedure leads to increased drain current, reduced efficiency, and increased power consumption and heat generation in the device, and finally, the heat generated by the part is damaged and breakdown occurs. Because the electric field has a direct effect on the ionization coefficient, by reducing the electric field around the gate, the ionization of atoms occurs at higher voltages, and this means that the breakdown voltage of the proposed structure has increased [23]. The maximum electric field that a material can withstand is called the critical electric field, which is closely related to the energy gap of the material. A material with a larger energy gap has a larger critical electric field and consequently a larger breakdown voltage. The critical electric field for silicon oxide is about 10 MV/cm, which is larger than that of silicon, 0.3 MV/cm.

Fig. 7 illustrates the 2D distribution of the electric field for V_{GS} = -5 V and V_{DS} = 10V. In the new device, an area of additional SiO_2 insulation is shaped between the gate and drain regions in a part below the gate. The presence of an insulator between the gate and drain as well as the existence of the SiGe layer reduces the accumulation of electric field points in the proposed structure relative to the basic structure and disperses the electric field lines in the channel. The reason for the scattering of field lines inside the channel of the new structure can be expressed based on the following continuity equation at the interface, which governs the common boundary between the silicon oxide region and the silicon channel [17].

$$E_{si} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} E_{ox} \qquad (3)$$

where ε_{ox} is the electrical permittivity for SiO_2 and ε_{si} is the electrical permittivity for Si. Because silicon has an electrical permittivity greater than oxide, therefore, according to Eq. (3), the electric field inside the oxide must be greater than the field inside the channel. As a result, the electric field lines are scattered inside the channel after passing the common surface between the two materials, which means a reduction of the electric field in the channel region and improving the breakdown point in the proposed device.

Fig. 8 shows the electric field lengthwise of the AA′ cutline at a distance of 25 nm from the surface for V_{GS} = - 5 V and V_{DS} = 10V which are compared in the proposed and basic structures. In the area where the oxide is



(a)

(b)

Fig.7. Two-dimensional distribution of electric field lines in basic structure (a) and proposed structure (b) for V_{GS} = -5V and V_{DS} = 10V.

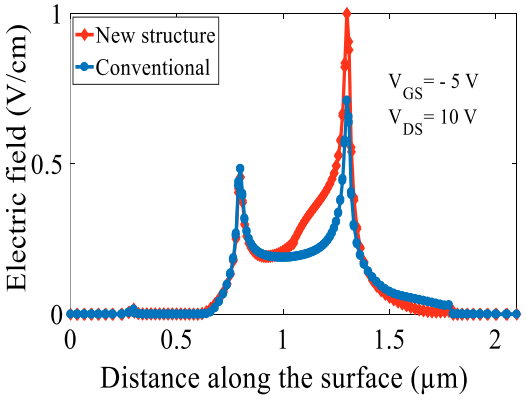


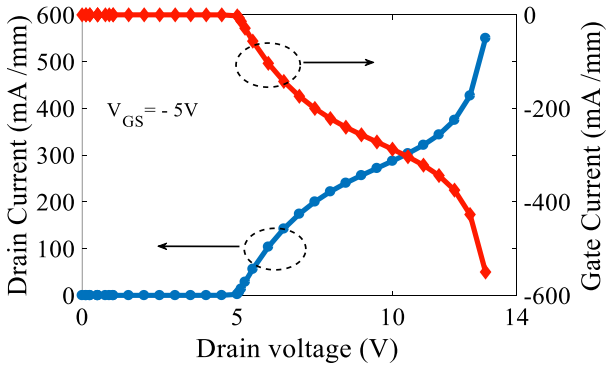
Fig. 8. Electric field profile at V_{GS} = - 5 V and V_{DS} = 10 along AA′ cutline for both structures.

located, an electric field peak is observed in the proposed structure. The critical electric field of oxide is larger than silicon, thus the larger electric field peak created in the proposed structure does not make a severe problem. So, it does not mean that the proposed structure reaches the breakdown point earlier. But also, according to the simulation results, the breakdown voltage of the new structure is improved.

Fig. 9 shows breakdown voltage characteristics in the basic structure (a) and the proposed structure (b). As can be seen from Fig. 9, for V_{GS} = - 5V, the breakdown voltage has increased from 13.5 volts in the basic structure to 18.5 volts in the new structure. The breakdown in the new device is improved by 37%.
The study of power in FETs can be done by following relation [19]:

$$P_{\max} = \frac{I_{Dsat}(V_{BR} - V_{Knee})}{8} \quad (4)$$

where I_{Dsat}, $V_{BR,}$ and V_{Knee} are the saturation current, breakdown voltage, and knee voltage, respectively.



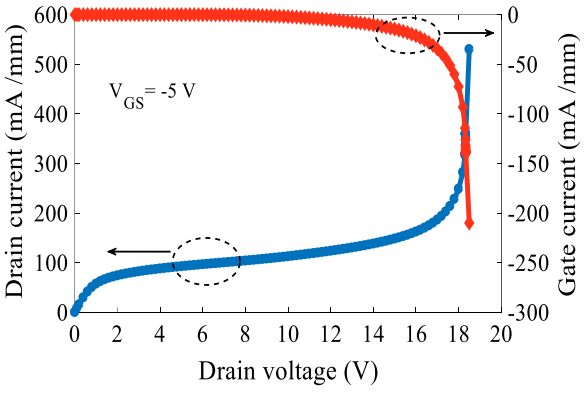


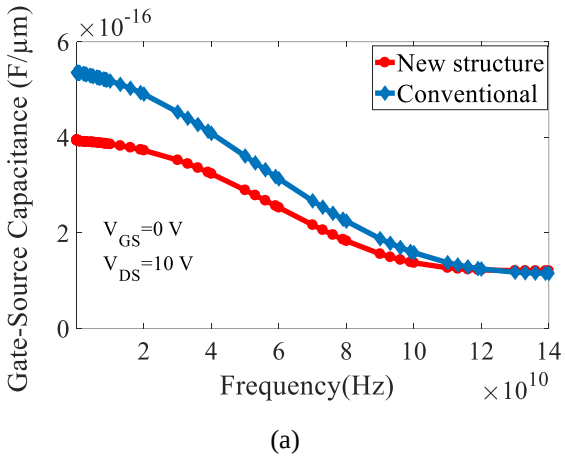
Fig. 9. Breakdown voltage characteristics for basic structure (a) and new structure (b) at V_{GS}= -5V.

In the new structure, two main characteristics of the device, breakdown voltage and drain current, have been improved simultaneously, therefore, the power density has been improved. The maximum output power in the new structure is 0.31W/mm, while for the base structure, it is 0.1 W/mm, which increases power density by 200%. Consequently, the new structure can be used in high-power applications.

IV. RF SIMULATION RESULTS

The parasitic capacitances of the source gate, C_{GS}, and the gate drain, C_{GD}, reduce the frequency performance of the transistor. In Fig. 10, C_{GS} and C_{GD} capacitances are shown for two structures in terms of frequency for V_{GS} = 0 V and V_{GD} = 10 V. The presence of an additional oxide box in the proposed structure channel, has caused a series capacitance, which reduces the capacities of C_{GS} and C_{GD}.

In Fig. 11 trans-conductance, g_m, of the structures at the bias of V_{GS} = 0 V and V_{GD} = 10 V are compared in terms of frequency.



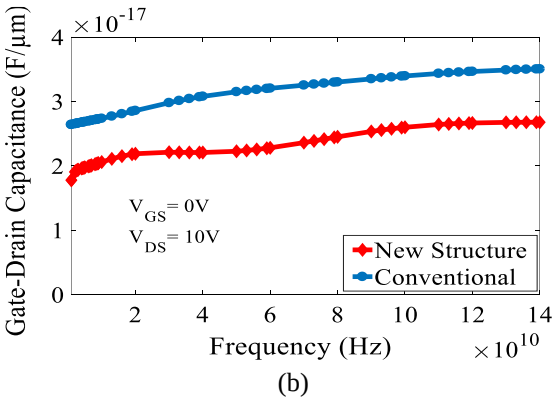


Fig. 10. Gate-source capacitance (a) and Gate-drain capacitance (b) of both the structures as a function of frequency for V_{GS} = 0V and V_{DS} = 10V.

Due to the insertion of SiGe as part of the channel inside the buried oxide, the effective channel width is increased and, because of the higher mobility of SiGe, the conductivity of the new device is improved compared to the basic structure. Fig. 12 shows the RF characteristics of structures including unilateral power gain (U), maximum available power gain (MAG), and current gain (h_{21}) as a function of frequency at the bias of V_{GS} = 0 V and V_{DS} = 10 V. The h_{21} has increased from 40 dB in the basic structure to 92 dB in the proposed structure, resulting in 130% improvement. In the case of the U, it also shows a significant improvement, where its value is 9.8 dB for the conventional structure and 18.2 dB for the proposed structure, which means an increase of 85%. The MAG has also improved from 14.5 dB in the basic structure to 24 dB in the proposed structure, showing a growth of 65%.

The cut-off frequency, denoted by f_T is a measure of the normal speed of the transistor without circuit constraints. It is the frequency at which the small signal gain of the current becomes one. The simulation shows that the cut-off frequency of the proposed structure is 18.5 GHz, which is better than the basic structure and is 17.8 GHz. The maximum oscillation frequency (f_{max}) is the maximum frequency at which the device still has power gain, and in fact, it is the maximum frequency for which the unilateral power gain becomes one. It is defined by the following relation [22].

$$f_{\max} = \frac{g_m}{4\pi C_{gs}} \sqrt{\frac{R_{DS}}{R_G}} \quad (5)$$

where g_m, the trans-conductance, is expressed by the following relation [22].

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}=const} \quad (6)$$

Also, R_{DS} is the resistance between the drain and source and R_G is the resistance of the gate, which increases with decreasing dimensions of the gate metal. The simulation shows that the f_{max} value has increased from 114.5 GHz in the basic structure to 118.5 GHz in the new structure. The main reason for the increase in the maximum oscillation frequency in the proposed structure is the increase in g_m due to the use of high electron mobility SiGe in the proposed structure, which also reduces the amount of C_{GS} and C_{GD} capacitances. The result is that the new structure is an appropriate option for high frequencies.

Table II shows the results of comparing the new structure with several structures. Comparison of structures should be done under the same conditions.

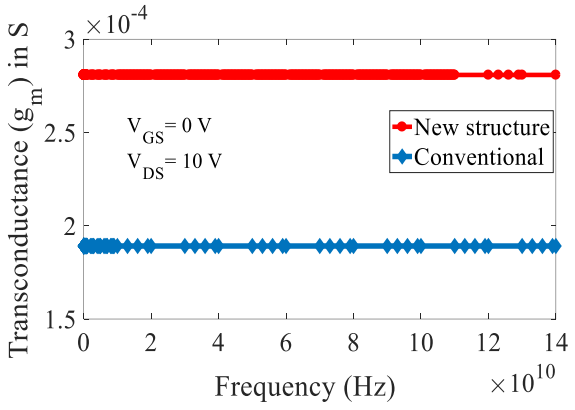


Fig. 11. Trans-conductance (g_m) of both structures as a function of frequency at V_{GS} = 0V and V_{DS} = 10V.

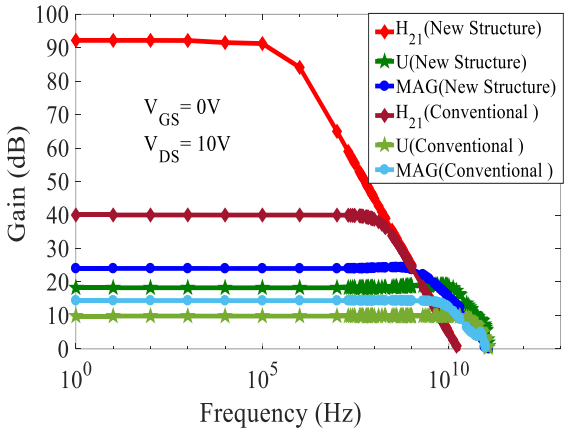


Fig. 12. H_{21}, U, and MAG as a function frequency for basic and proposed structures at V_{GS} = 0 V and V_{DS} = 10 V.

TABLE II
The Comparison Between New Structures and Other Structures.

Article	DCR [14]	SO-ED [24]	INL-SOI [3]	This work
Breakdown voltage (V_{GS}= -5V)	14.5V	16.1V	12.5V	18.5V
Current (V_{GS}=0.5V , V_{DS}=5V)	228 mA/mm	300 mA/mm	265 mA/mm	300 mA/mm
f_T (V_{GS}=0V , V_{DS}=10V)	16.5 GHz	18.5 GHz	12.5 GHz	18.5 GHz
f_{max} (V_{GS}=0V, V_{DS}=10V)	59.2 GHz	65.2 GHz	21 GHz	118.5 GHz
H_{21} (V_{GS}=0V, V_{DS}=10V)	38 dB	34 dB	51.5 dB	92 dB
U (V_{GS}=0V, V_{DS}=10V)	8.7 dB	12 dB	4 dB	18.2 dB
MAG (V_{GS}=0V, V_{DS}=10V)	13.1 dB	14 dB	8 dB	24 dB
transistor dimensions	2.5*0.7 μm²	2.1*0.7 μm²	2.1*0.7 μm²	2.1*0.7 μm²

This means that in all structures, the dimensions of the device, bias points, and models activated in the simulator are identical. According to the table, almost all results of the proposed structure are better than the other structures. This indicates that the new structure is a suitable structure with improved DC and RF specifications.

V. OPTIMIZATION AND DIMENSIONS

This section includes optimizing and determining the size of the proposed structure dimensions to obtain the best results of simulation. It is noteworthy that the dimensions of the SiGe region and the oxide between the gate and drain have been determined and optimized after several simulations. The values and parameters that are optimized here are four parameters, *L*, *W*, *H*, and *T* in 4 optimization phases. To perform it, one of these parameters is changed at each step while the others are fixed. After the proper assessment of a variable, its amount is fixed in succeeding phases. Breakdown voltage, saturation current, maximum oscillation frequency, current gain, cut-off frequency, and unilateral power gain of the device are considered evaluation characteristics. Fig.13 (a) and (b) show the optimization process for the length (L) and width (W) of the oxide box region in the channel, respectively. As can be seen, the proper length value is L= 0.75µm and for W is 0.06 µm. Other parameters, such as *T* and *H*, have been optimized and determined in a similar way, where their values are selected to be 1.5µm and 0.07µm, respectively.

VI. CONCLUSION

In this paper, the DC and RF specifications of the proposed structure are examined and its results are compared with the basic structure. Adding SiGe region to the buried oxide zone of the channel, due to its properties such as high mobility of carriers, high speed, and excellent frequency performance has increased the drain current. Also, by adding an extra oxide zone between the gate and drain and below a part of the gate zone and controlling the critical electric field that occurs at the gate corner close to the drain, it has increased the breakdown voltage of the new device. So the breakdown voltage has significantly improved from 13.5 volts to 18.5 volts, Also, the drain current in the proposed structure shows a 120% increase compared to the basic structure. This has increased the P_{max} from 0.1 W/mm in the basic structure to 0.31 W/mm in the proposed structure, resulting in a P_{max} of 200% increase in the new structure. Also, due to the reduction of load in the channel, the frequency characteristics of the new structure such as h_{21}, U, and MAG have been improved by 130%, 85%, and 65%, respectively. It is noteworthy that the f_{max} has been upgraded from 114.5 GHz in the basic structure to 118.5 GHz in the new structure. According to the specification obtained for the suggested structure, this device can be used in requests with high power and frequency.

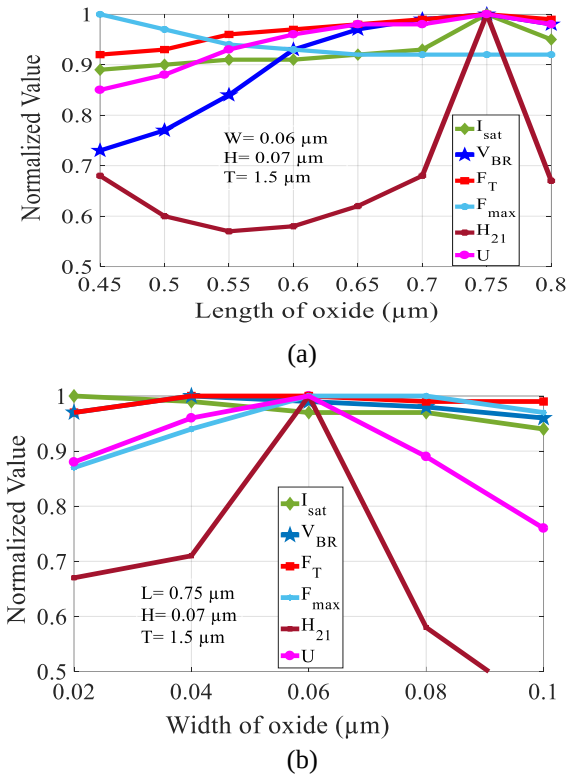


Fig. 13. Optimization process for (a) oxide length and (b) oxide width.

VII.REFERENCES

[1] J. Ervin, A. Balijepalli, P. Joshi, V. Kushner, J. Yang, and T. J. Thornton, "CMOS compatible SOI MESFETs with high breakdown voltage," IEEE Trans. Electron Devices, vol. 53, no. 12, pp. 3129–3134, 2006.

[2] G. Manes, and G. Pelosi, "Enrico Fermi's IEEE Milestone in Florence: For his Major Contribution to Semiconductor Statistics," Firenze University Press, Vol. 2, pp. 1924 – 1926, 2015.

[3] H. Shahnazarisani, and A.A. Orouji. "A Novel SOI MESFET by Implanted N Layer (INL-SOI) for High-Performance Applications," Modeling and Simulation in Electrical and Electronics Engineering, vol.1, no.1, pp. 7-12, 2021.

[4] A.A. Orouji, Z. Ramezani, and A.A. Heydari, "A novel high - performance SOI MESFET by stopping the depletion region extension," Superlattices and microstructures, vol. 75, p. 195 – 207, 2014.

[5] L. Pu, L. Yan, & W. Hanlei, "Introducing a buried pure silicon layer in SOI-MESFET transistor to increase the breakdown voltage by modifying carriers and electric field distribution," Emergent Materials, pp. 1-7, 2023.

[6] Antonio Di Bartolomeo, "Graphene Schottky diodes: An experimental review of the rectifying graphene/semiconductor heterojunction," Physics Reports, 2016, vol. 606, P. 1-58.

[7] JP. Colinge, "Silicon-On-Insulator Technology Materials to VLSI," Kluwer Academic Publishers, 2004, pp.203-298.

[8] Z. Ramezani and A. A. Orouji, "Improving Self-Heating Effect and Maximum Power Density in SOI MESFETs by Using the Hole's Well

Under Channel," in IEEE Transactions on Electron Devices, vol. 61, no. 10, pp. 3570-3573, Oct. 2014.
[9] J. - P. Colinge, "Thin-film SOI technology: The solution to many submicron CMOS problems," in International Technical Digest on Electron Devices Meeting, 1989, IEEE.
[10] A. Aminbeidokhti, A. A. Orouji, S. Rahmaninezhad, and M. Ghasemian, "A Novel High-Breakdown-Voltage SOI MESFET by Modified Charge Distribution," in *IEEE Transactions on Electron Devices*, vol. 59, no. 5, pp. 1255-1262, May 2012.
[11] L. Abid, I. Hadjoub, A. Doghmane, N. E. Abdaoui, & Z. Hadjoub, "A Novel Silicon on Insulator MESFET with Multi-∏ Regions to Improve DC and RF Performances," Silicon, pp. 1-13, 2022
[12] A. Naderi, and H. Mohammadi, "Shifted gate electrode of silicon on insulator metal semiconductor FETs to amend the breakdown and transconductance," The European Physical Journal Plus, vol. 136, no. 6, p. 1-17,2021.
[13] E. Farahzad, & A. Naderi, "Embedded metal and L-shaped oxide layers in silicon on insulator MESFETs: higher electric field tolerance and lower high frequency gate capacitances," Journal of Materials Science: Materials in Electronics 33, no. 25, pp. 19971-19984, 2022.
[14] MK. Anvarifard, "Symmetrical SOI. MESFET with a dual cavity region (DCR-SOI MESFET) to promote high-voltage and radio-frequency performances," Supperlattices and Microstructtures, vol. 98, p. 492–503,2016.
[15] Hossein Mohammadi, Huda Abdullah, Chang Fu Dee and P. Susthitha Menon, "A modified two- dimensional analytical model for short-channel fully depleted SOI MESFET's," Microelectronics Reliability, Volume 83, Pages 173-179, 2018
[16] H. Shahnazarisani, A.A. Orouji, and M.K. Anvarifard, "A novel SOI MESFET by π-shaped gate for improving the driving current," J Comput Electron, vol. 13**,** pp.562–568, 2014.
[17] B. Fath Ganji, A. Mir, A. Naderi, R. Talebzadeh, A. Farmani,"Enhanced performance of SOI MESFETs by displacement of gate contact and applying double oxide packets," Electrical Engineering, pp. 1-14, 2023.
[18] H. Mohammadi, H. Abdullah, Chang Fu Dee, P. Susthitha Menon, "A modified two dimensional analytical model for short-channel fully depleted SOI MESFET's," Microelectronics Reliability, Volume 83, Pages 173-179, 2018.
[19] M. Mohtaram, A. A. Orouji, Z. Ramezani, & D. Keighobadi, "Physical Analysis on the DC and RF Operations of a Novel SOI-MESFET with Protruded Gate and Dual Wells," Silicon, pp. 1-7, 2021.
[20] M.K. Anvarifard, "An impressive structure containing triple trenches for RF power performance (TT - SOI - MESFET)," Journal of Computational Electronics, vol.17, no. 1, p. 230 – 237, 2018.
[21] M. Khoorabeh, A.A. Orouji, and Dariush Madadi. "Improvement of a novel SOI-MESFET with an embedded GaN layer for high-frequency operations." Silicon pp. 1-8, 2021.
[22] H. Shahnazarisani, and A.A. Orouji. "A Novel MESFET structure by U-shape buried oxide for improving the DC and RF Characteristics." Superlattices and Microstructures, vol. 82, pp. 55-66, 2015.
[23] M. Mohtaram, A.A. Orouji, and Z. Ramezani, "A Novel SOI MESFET to Improve the Equipotential Contour Distributions by Using an Oxide Barrier," Silicon, vol. 11, p. 879–889, 2019.
[24] A. Naderi, F. Heirani, "A novel SOI-MESFET with symmetrical oxide boxes at both sides of gate and extended drift region into the buried oxide," AEU - International Journal of Electronics and Communications, Volume 85, Pages 91-98, 2018.
[25] S. Khanjar, A. Naderi, "DC and RF characteristics improvement in SOI-MESFETs by inserting additional SiO2 layers and symmetric Si wells," Materials Science and Engineering: B, Volume 272, 115386, ISSN 0921-5107, 2021.
[26] M. Mohtaram, and A.A. Orouji, "A novel SOI MESFET to spread the potential contours towards the drain," International Journal of Electronics, vol. 107.9, p. 1506-1523, 2020.
[27] A. Naderi, K.M. Satari, and F. Heirani, "SOI – MESFET with a layer of metal in buried oxide and a layer of SiO2 in channel to improve RF and breakdown characteristics," Materials Science in Semiconductor Processing, vol. 88, p. 57 - 64. 2018.
[28] A. Naderi, and H. Mohammadi, "High breakdown voltage and high driving current in a novel silicon-on-insulator MESFET with high- and low-resistance boxes in the drift region," Eur. Phys. J. Plus, vol. 133**,** no. 221, 2018.
[29] J. Zhang, X. Jin, P.-H. Tsien, and T.-C. Lo, "Cross-sectional transmission electron microscopy study of Si/SiGe heterojunction bipolar transistor structure grown by ultra-high vacuum chemical vapor deposition," Jpn. J. Appl. Phys., vol. 36, no. 7B, pp. 903–905, 1997.
[30] S.C. Jain, M. Willander, "Silicon-Germanium Strained Layers and Heterostructures: Semi-conductor and semi-metals series," Elsevier, Volume 74, Pages 1-308, 2003.
[31] Atlas, Device Simulator, "Atlas user's manual," Silvaco International Software, Santa Clara, 2015.
[32] M. Bruel, B. Aspar, A. Auberton-Herve, "Smart-cut: a new silicon on insulator material technology based on hydrogen implantation and wafer bonding", Jpn J Appl Phys, 1997;36:1.