Dual-Channel Indium Nitride Tunnel Field Effect Transistor: A Comprehensive Study on Design, Sensitivity, and Electrical Performance

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***Abstract*— This paper presents a vertical tunnel field effect transistor (TFET) that incorporates two parallel side wall channels. The channel material utilized in this design is Indium Nitride (InN), which is sandwiched between lateral gates. This configuration allows for the amplification of drive current through extended tunneling area, taking advantage of the benefits offered by the vertical structure. InN is a promising channel material due to its high electron mobility and high electron velocity, which enhances the device performance. The impact of critical design parameters on the device performance is comprehensively assessed. The optimal values of a 2D variation matrix of threshold voltage and on-state current can be determined by considering the variation of gate workfunction and source doping density, which are two crucial design measures. Additionally, a statistical analysis is carried out to evaluate the sensitivity of the device main electrical parameters with respect to the variation of critical design parameters. The findings indicate that the device attains a current of 1 mA when in the on-state, with an on/off current ratio of 1.3×1010. Additionally, it exhibits an average subthreshold swing of 20 mV/dec, and maximum subthreshold swing of 4.8 mV/dec, leading to reduced power consumption and enhanced switching speeds.**

***Index Terms*— Band to Band Tunneling; Subthreshold Swing; Vertical Tunnel Field Effect Transistor; Gate Workfunction.**

I. INTRODUCTION

The continuous demand for higher integration densities and faster processing speeds in modern electronics has led to the scaling down of MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) dimensions. However, this scaling has resulted in the emergence of short-channel effects, such as drain-induced barrier lowering and subthreshold leakage, which degrade the device performance and reliability [1-2]. To overcome these challenges, tunnel field-effect transistors (TFETs) have been proposed as a potential candidate for conventional MOSFETs due to several unique features [3-6]. In conventional MOSFETs, carriers are transported through a gate-modulated potential barrier. The subthreshold swing (SS), defined as the minimum change in gate voltage required to achieve a certain change in drain current, is a crucial parameter that determines the device switching performance. The subthreshold swing of MOSFETs is limited by thermionic emission, resulting in a minimum value of approximately 60 mV/dec at room temperature. In contrast, TFETs operate based on a different current transport mechanism, i.e., tunneling of carriers through a gate-modulated barrier width via band-to-band tunneling. This mechanism results in a subthreshold swing less than 60 mV/dec at room temperature, making TFETs a promising candidate for future low-power applications. Nevertheless, TFETs encounter a significant obstacle as a result of their limited drive current. The primary cause of this phenomenon can be primarily ascribed to the restricted tunneling junction located at the boundary between the source and channel regions. Various methods, such as material engineering, structure engineering, and doping engineering, have been employed to enhance the efficiency of TFET. The utilization of III-V materials in heterojunction TFETs has proven to be particularly advantageous, as it offers significant improvements in device performance owing to their low effective mass and high lattice matching [7-10]. Furthermore, the utilization of the line tunneling mechanism has been implemented in various TFET structures such as vertical TFET [11-14], L-shaped [15-16], F-shaped [17-18], and electron-hole bilayer TFET [19-21], and electrically doped SiGe TFET [22]. This technique aims to enhance the tunneling area, although it necessitates a complex fabrication process for some of these structures. Another effective approach is pocket doping, which serves to amplify the electric field at the tunneling interface. Consequently, this augmentation facilitates an increase in the tunneling rate. Pocket doping is characterized by the presence of a high density of dopants, with a polarity distinct from that of the source dopant, localized within a confined region at the interface of the source-channel junction. The incorporation of a negative capacitance gate insulator within a nanowire configuration greatly improves the efficiency of the field effect transistor [23]. This advancement holds potential for its application in TFETs to amplify the drain current. The limitations associated with physical doping have led to the introduction of electrically doped structures as a more effective method for generating the necessary charges in the source region [24].

In this paper, a vertical TFET structure is proposed with two parallel side wall channels using Indium Nitride (InN) as the channel material. The author has conducted an investigation on the vertical FET based on silicon in a previous study [25]. However, the proposed structure offers several unique advantages that makes it a novel and promising device for future nanoelectronics applications. Firstly, the use of InN as the channel material results in a lower subthreshold swing and a higher tunneling probability due to its lower effective mass and higher mobility. This leads to a significant improvement in

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the device switching speed. Secondly, the extended source region increases the tunneling window and results in higher on-state currents. Thirdly, the use of two side wall channels further improves the device performance by providing additional tunneling paths and reducing parasitic capacitance Basically, in a conventional horizontal TFET, the parasitic capacitance is primarily due to the gate-drain and gate-source overlap capacitances, which can be large due to the relatively large gate-drain and gate-source spacing. In contrast, in a vertical TFET, the gate is placed above the channel, which reduces the gate-drain and gate-source spacing significantly. This results in a significant reduction in the parasitic capacitance, as the overlap capacitances are reduced due to the smaller gate-drain and gate-source spacing. The impact of various physical and structural design parameters on the device performance is comprehensively assessed. In addition, a statistical analysis is carried out to analyze the sensitivity of the device main electrical parameters, such as the off-state current, on-state current, threshold voltage, and subthreshold swing, with respect to the variation of the design parameters. The coefficient of variation in percentile is calculated to quantify the sensitivity of each parameter. By definition, coefficient of variation provides a measure of the relative variability of a parameter and can be used to identify the most critical design parameters that need to be tightly controlled during the fabrication process. The paper is structured in the following manner: the subsequent section introduces the device structure and simulation models. Subsequently, a comprehensive assessment is conducted to determine the impact of critical physical and structural design parameters on the device performance. Finally, the conclusion section wraps up the paper.

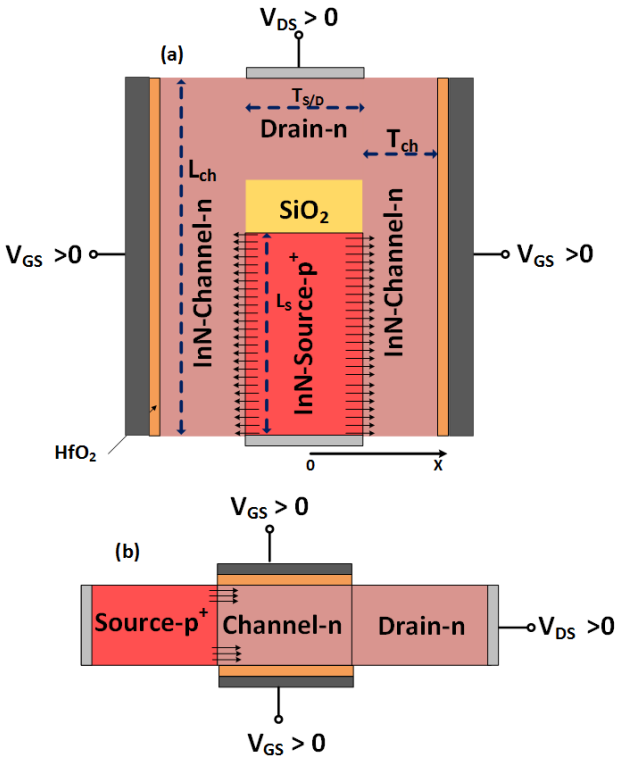

Fig. 1. 2D schematics of (a) Dual Channel Vertical TFET (DCVTFET) and (b) conventional double gate TFET. The homojunction structure is designed based on InN.

II. DEVICE STRUCTURE, SIMULATION SET UP AND OPERATION

Fig. 1(a) and 1(b) depict the 2D schematics of the Dual Channel Vertical TFET (DCVTFET) and conventional double gate TFET, respectively. The proposed DCVTFET structure exploits an extended source region situated at the interface of the two side wall channels to enhance the tunneling rate and improve the drive current.

Table I presents the initial design parameters for the proposed devices. In order to accurately evaluate the performance of the DCVTFET, numerical simulations are conducted using the ATLAS device simulator [26] with the following models being activated: (a) Band to Band Tunneling; The main mode of operation of the DCVTFET device is the quantum band to band tunneling through a tunneling window found in between the n^+ and p^+ regions at the interface of the source and channel regions. The nonlocal band to band tunneling model takes into account the gate modulated tunneling of carriers from the source valence band to the channel conduction band. (b) Mobility Models; In principle, the mobility of carriers at higher electric fields is subject to field-dependent parameters, leading to a decrease in mobility as the electric field increases. This can be attributed to increased lattice scattering at higher carrier energies. Consequently, in the calculation of drain current, the effects of both horizontal and vertical electric fields on carrier mobility are taken into consideration. Furthermore, when it comes to higher doping concentrations, there is a decrease in the mobility of both electrons and holes due to ionized impurity scattering. In the simulation models employed for DCVTFET, the impact of doping density on carrier mobility is included, owing to the presence of heavily doped tunneling regions. (c) Trap Assisted Tunneling; Trap-assisted-tunneling (TAT) is essentially a mechanism that involves the generation of band to band tunneling current by the contribution of phonons. The TAT mechanism generates a leakage current prior to the onset of band to band tunneling, which results in a significant degradation of the turn-on characteristic and subthreshold swing of the DCVTFET. Consequently, a thorough understanding of TAT is crucial in the development of DCVTFETs with improved performance. (d) Bandgap Narrowing Model; Experimental observations have indicated that an increase in impurity concentration leads to a reduction in the bandgap, a phenomenon referred to as bandgap narrowing effect. This effect is attributed to the formation of an impurity band, which arises from the overlapping of impurity states. In the proposed DCVTFET device that comprise adjacent dual channel layers and heavily doped source region with different doping density, alterations in the conduction band minimum and valence band maximum due to the doping density may significantly impact the tunneling rate. (e) Quantum Confinement Model; The proposed DCVTFET involves the formation of a tunneling junction within a quantum well structure that is formed along the thickness of the channel. Importantly, when the channel thickness is scaled, the energy of sub-bands may increase, potentially altering the density of states. Therefore, models that consider the effects of quantum confinement are utilized in order to address this phenomenon. The simulated result is compared with a fabricated device in reference [27], which has a silicon channel thickness of 13nm,

in order to calibrate the models and parameters as illustrated in Fig. 2. The manufacturing process of the device that is compatible with the proposed Si-based device in [27] can be outlined as follows: initially, the source electrode is deposited on the substrate material through sputtering. Subsequently, to establish the vertical structure, an InN layer is cultivated using an epitaxial process. This is followed by the formation of a p^+ InN layer through ion implantation technique. Then, an insulating SiO_2 region is grown via epitaxial process to insulate the source and the drain region. After the growth of the epitaxial layer, the vertical active layers and the drain region are patterned using i-line photolithography. The vertical structure is then formed through selective epitaxial growth. Upon the creation of a gate dielectric, HfO_2, via atomic layer deposition, NH_3 plasma treatment is conducted to generate an HfON interfacial layer. The HfON interfacial layer exhibits superior interface properties and higher permittivity. Lastly, the sidewall gate electrodes and the drain electrodes are produced through sputtering.

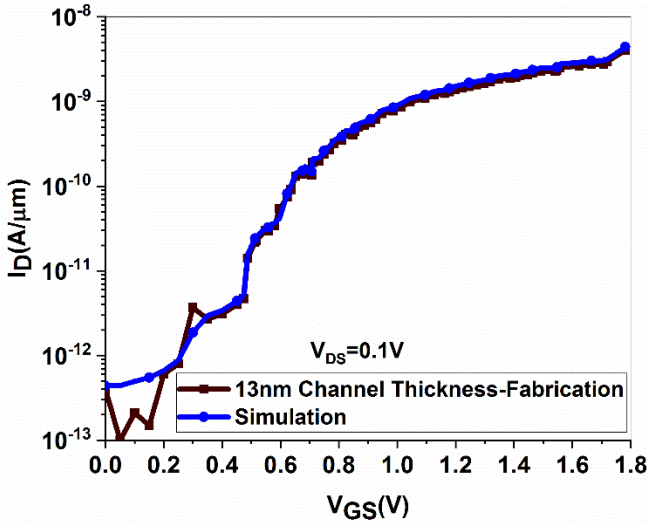

Fig.2: Transfer characteristics of simulated DCVTFET with the device fabricated in [27]. The drain bias is V_{DS}=0.1V.

TABLE I
Primitive Design Parameters for the DCVTFET.

Parameters	DCVTFET
Channel Length (L_{ch})	60 nm
Extended source length(Ls)	30 nm
Channel thickness (T_{ch})	5 nm
Gate insulator thickness-HfO_2	2 nm
Source doping density	3×10^{19} (cm^{-3})
Channel and Drain doping density	1×10^{18} (cm^{-3})
Gate Work Function (WF_G)	5.3 eV
Source and Drain thickness	5 nm
Length of SiO_2	10 nm

III. RESULTS AND DISCUSSIONS

The operational principle of the DCVTFET that has been suggested relies on the phenomenon of band to band tunneling occurring at the interface between the source and channel regions. The energy band bending occurring at the interface between the source and channel regions can be effectively estimated through the utilization of a barrier that resembles a triangle in shape. Employing the Wentzel-Kramers-Brillouin approximation (WKB), it becomes possible to describe the tunneling probability (T_{WKB}) of the DCVTFET as follows:

$$T_{WKB} \approx exp(-\lambda \frac{4\sqrt{2m^*}E_G^{3/2}}{3q\hbar(E_G+\Delta\Phi)}) \quad (1)$$

The tunneling length, denoted by λ, signifies the extent of the transition region at the interface between the source and channel regions. The bandgap energy of the source region is represented by E_G, while $\Delta\Phi$ represents the tunneling window where band-to-band tunneling (BTBT) is permitted. Essentially, a smaller value of λ indicates a greater band bending at the tunneling region. The tunneling probability, T_{WKB}, can be controlled by increasing the gate bias, which reduces λ and simultaneously enlarges the $\Delta\Phi$ window. To enhance the operational efficiency of DCVTFET, it is crucial to meticulously design the tunneling junction to ensure a high BTBT rate and excellent gate controllability across the tunneling barrier. The proposed device employs two parallel channel with extended tunneling region that improves the tunneling current. The energy band diagram of the device is depicted in Fig.3, showcasing the transition from source to channel in the lateral direction, both in the off-state and on-state. It is apparent that in the off-state, the tunneling barrier is wide, effectively impeding the passage of carriers through tunneling. Nevertheless, with a significant increase in the gate bias, the band bending phenomenon takes place, enabling band to band tunneling to occur.

In Fig. 4, a comparison is presented between the simulated transfer characteristics of a conventional TFET and a DCVTFET. The analysis reveals that the DCVTFET exhibits a distinct step-like behavior in its drain current profile. The threshold voltage of the device is defined as the gate voltage required for the bands to overlap, indicating the voltage necessary for the device to transition from a low off-state drain current to high conductance. The electrical characteristics of the devices under investigation are summarized in Table II. The results demonstrate that the DCVTFET device has achieved a significantly higher on-state drive current (18 times higher than the conventional TFET) and improved switching speed. These enhancements can be attributed to the presence of sidewall parallel channels and a larger source and channel overlap area, facilitating tunneling transmission, as compared to the conventional lateral TFET. The subthreshold swing of the device is determined using two different approaches. The first method involves calculating the inverse of the maximum slope in the transfer characteristic, resulting in a subthreshold swing of 4.8 mV/dec for the DCVTFET. On the other hand, the second method calculates the average subthreshold swing based on the necessary gate voltage variation to achieve a 106 variation in the drain current. According to this method, an average subthreshold swing of 20 mV/dec is attained for the proposed device.

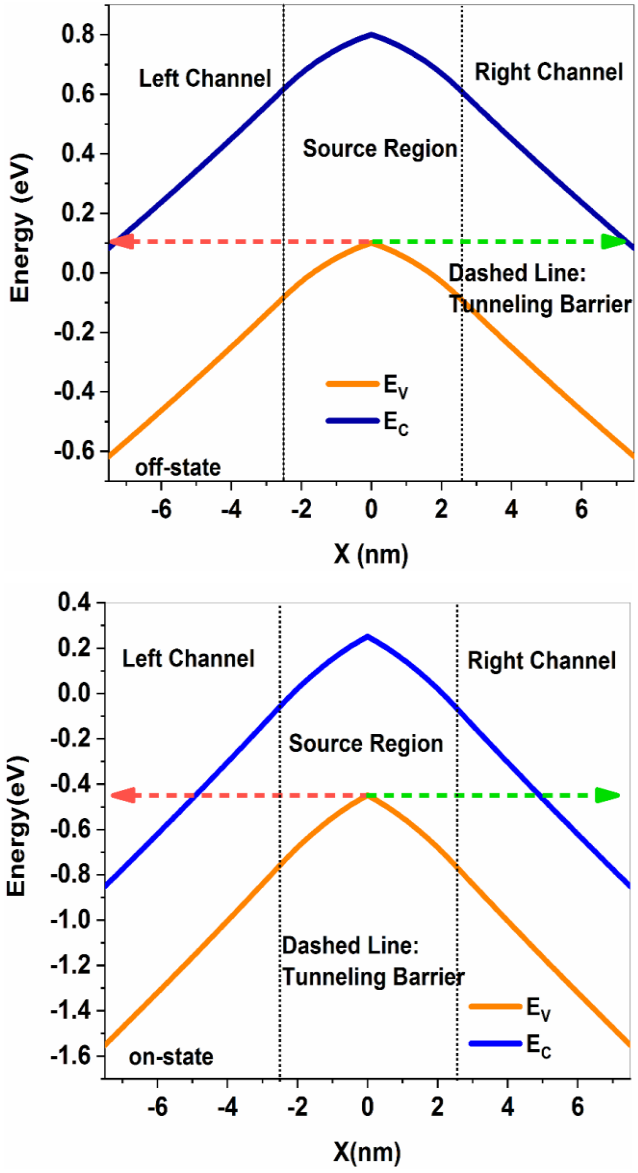

Fig. 3. Energy band diagram of DCVTFET in the off-state and on-state.

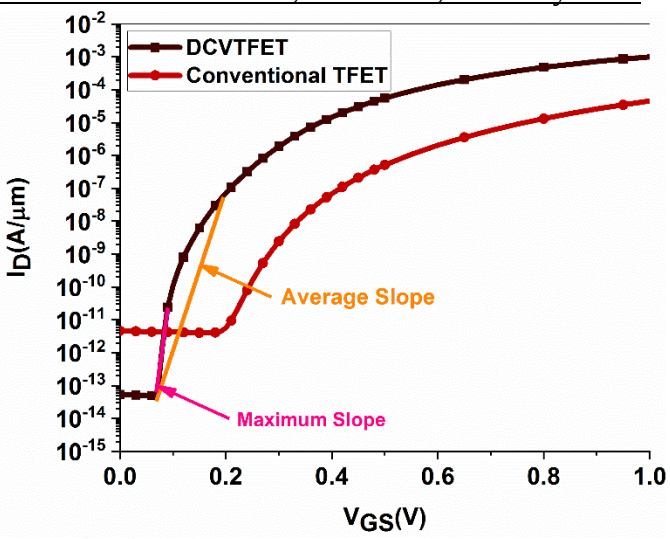

Fig. 4. Transfer characteristics of DCVTFET and conventional TFET

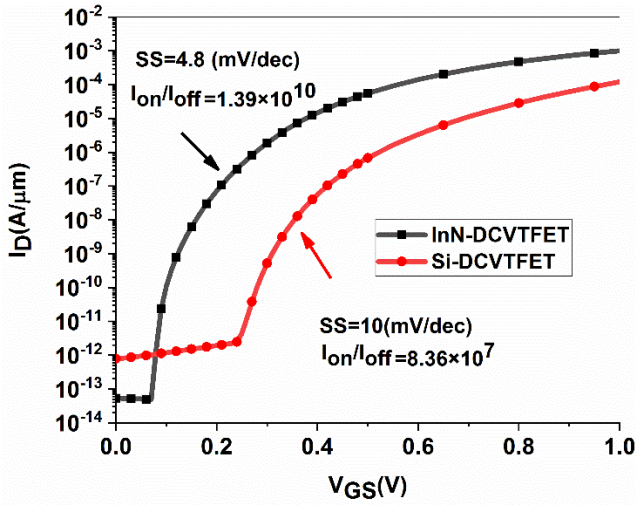

Fig. 5: Transfer characteristics of InN-DCVTFET and Si-DCVTFET.

TABLE II
Main Electrical Parameters of DCVTFET and Conventional TFET

Device	**I_{on} (A/μm)**	**I_{off} (A/μm)**	**V_{th} (V)**	**SS mV/dec (maximum slope)**	**I_{on}/I_{off}**
DCVTFET	8.18×10^{-4}	5.98×10^{-14}	0.07	4.8	1.39×10^{10}
Conventional TFET	4.52×10^{-5}	4.62×10^{-12}	0.21	15	9.78×10^{6}

Fig. 5. depicts the transfer characteristics of InN-DCVTFET and Si-DCVTFET, allowing for a comprehensive comparison. One notable attribute of InN is its significantly lower carrier effective mass, which enhances the efficiency of tunneling current when compared to silicon. The findings clearly indicate that InN achieves a maximum subthreshold swing of 4.8 mV/dec, outperforming the silicon material which achieves 10 mV/dec.

Fig .6. depicts the impact of the vertical length of the source on the on-state and of-state current. The findings indicate that with an increase in the source length, the tunneling window expands. Consequently, the lateral line-tunneling along the interface of the source and channel region leads to a rise in the on-state current. It is important to highlight that there is no fluctuation in the off-state current. This phenomenon can be primarily attributed to the presence of an oxide region integrated between the source and region, which offers significant protection against the DIST effect.

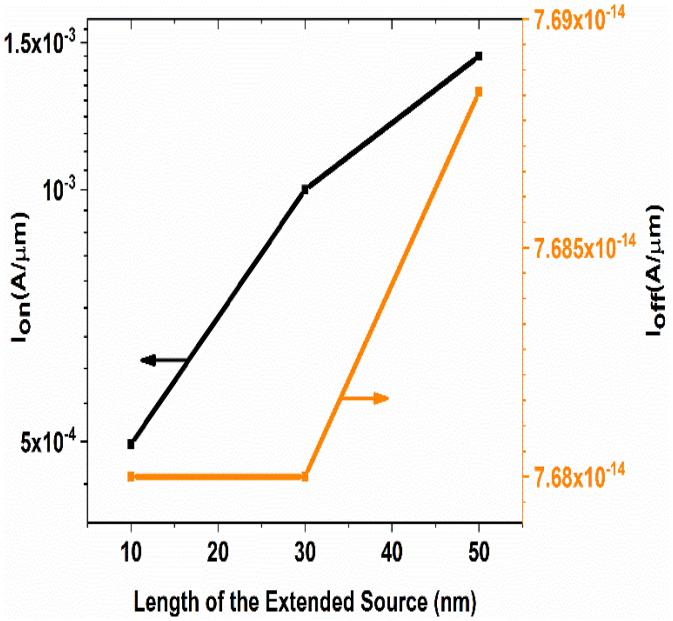

Fig. 6. Impact of length of the vertical extended source region on the on-state and off-state current of the proposed DCVTFET.

The workfunction of gate material is a crucial design parameter that is responsible for tuning the band to band transition voltage in DCVTFET. The transfer characteristics of the device are depicted in Fig.7, wherein the gate workfunction value is parametrized. The findings indicate that the on-state current and required voltage for onset of band to band tunneling are significantly altered depending on the specific gate electrode material utilized. As the gate workfunction decreases towards 4.8 eV, a lateral shift of the I_D-V_{GS} curves to the left is observed. The occurrence of band to band tunneling requires a perfect overlap of electron and hole wave functions within a short tunneling barrier. The results indicate that as the workfunction difference between the gate and the underlying channel decreases, the electrically induced electron density in the channel increases. This accumulation of high electron density in the channel leads to a lower tunneling distance and a lower gate bias for the transition of drain current from minimum off-state current to high saturation value.

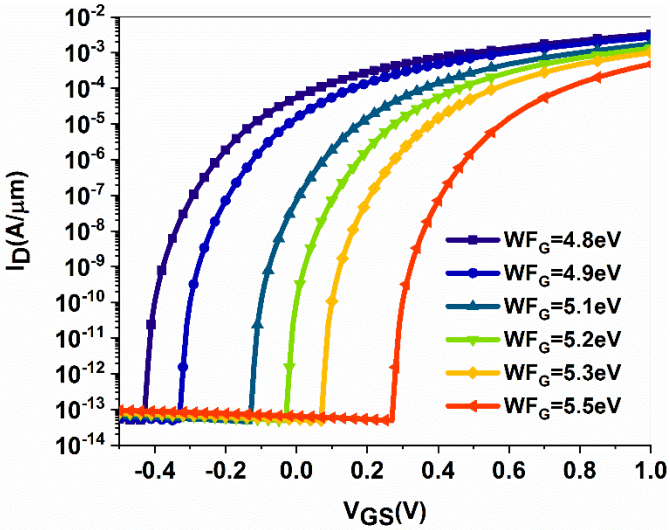

Fig. 7. Transfer characteristics of the proposed DCVTFET as the workfunction of the sidewall gates is parametrized.

Fig .8. depicts the influence of the doping density of the source region on the transfer characteristics of the DCVTFET. Fundamentally, the initiation of tunneling necessitates a step p^+-n^+ tunneling junction. The outcomes showcase that the on-state current, threshold voltage, and subthreshold swing are heavily reliant on the doping density of the source. Essentially, in DCVTFET, high source doping is imperative as it diminishes the width of the tunneling barrier, thus facilitating high electric fields that are crucial for generating sufficient tunneling currents. It is noteworthy to emphasize that the relationship between the optimal source doping and the effective density of states is a fundamental aspect that must be taken into account in the design of TFETs.

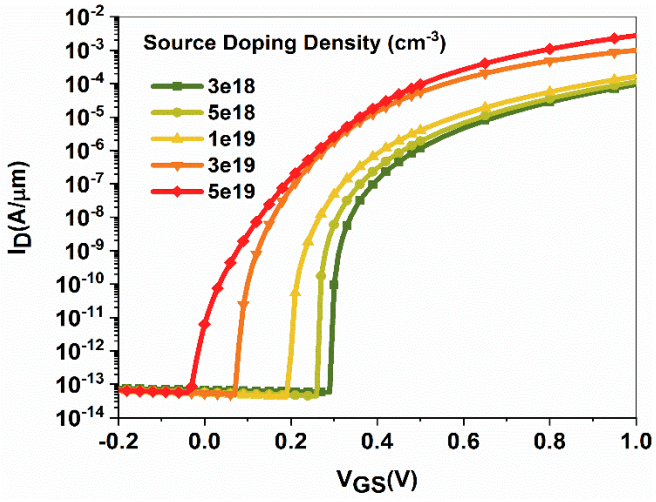

Fig. 8. Impact of extended source doping density on the transfer characteristics of the proposed DCVTFET.

The findings indicate that the tunneling rate is greatly influenced by the opposite charge density at the tunneling junction in the source and channel region, owing to the wide tunneling window. Moreover, the gate workfunction and source doping density are identified as crucial design parameters that significantly impact the tunneling rate. To assess the variation in on-state current and threshold voltage, a 2D variation matrix

is computed by altering the gate workfunction and source doping density. Analyzing the on-state current variation, as illustrated in Fig. 9 (a), it is evident that the maximum on-state current can be attained in the top left corner of the variation matrix. This region corresponds to a heavily doped source region and a low gate workfunction value, ultimately resulting in a steep p^+-n^+ tunneling junction. However, in order to achieve a higher on-state current, it is necessary to have a low positive gate bias for the initiation of tunneling. The 2D variation matrix shown in Fig. 9 (b) illustrates the changes in the threshold voltage as the gate workfunction and source doping density are adjusted. The negative threshold voltage, located in the top left corner of the contour, is a result of a heavily doped source region and a low gate workfunction value, which facilitates the accumulation of electrons in the channel. Conversely, in the bottom right corner of the contour, a high positive threshold voltage can be obtained, leading to a reduction in the on-state tunneling current. This effect is primarily attributed to the low source doping density and a high value of the gate workfunction, which simultaneously increases the tunneling barrier. To ensure proper device operation, it is crucial to find the appropriate combination of source doping density and gate workfunction that results in the lowest possible positive threshold voltage.

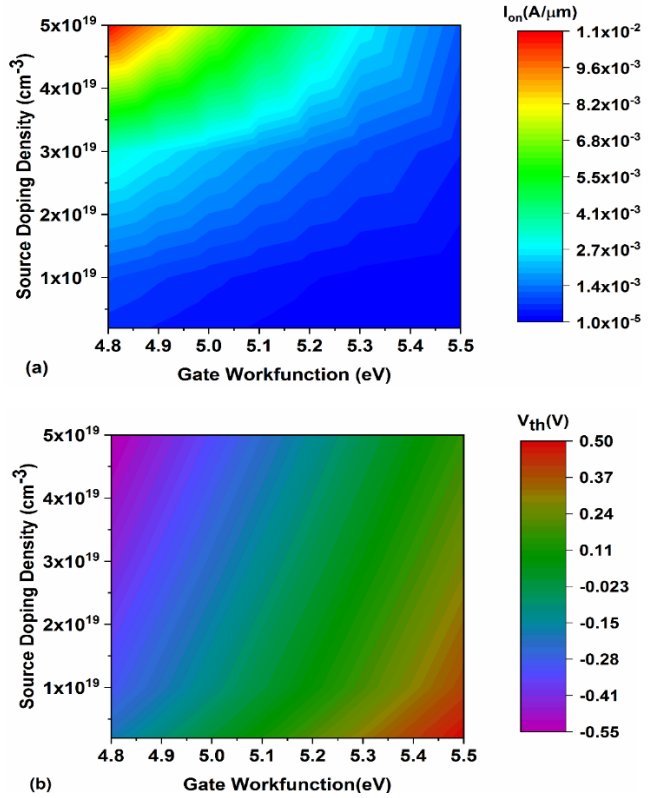

Fig. 9. 2D variation contour of (a) on-state current and (b) threshold voltage as a function of source doping density and gate workfunction.

The channel charge density and threshold voltage in a device are influenced by two key factors: the gate workfunction and the channel doping density. By analyzing the variation of these two factors, a 2D matrix of threshold voltage can be calculated, depicted in Fig. 10. In the case of n-type operation, a low positive voltage is necessary. The findings indicate that the threshold voltage is more significantly affected by changes in the gate workfunction rather than the channel doping density. Specifically, when the gate workfunction exceeds 5.3eV and a moderately low doped channel is utilized, it is possible to achieve near zero positive gate bias for the onset of tunneling.

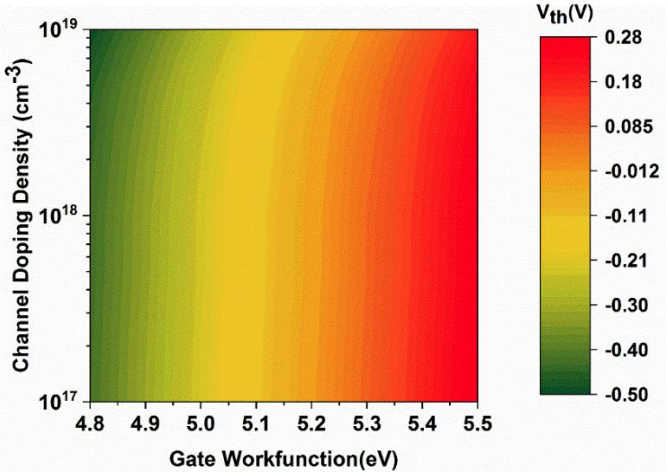

Fig. 10. 2D variation contour of threshold voltage versus variation of channel doping density and gate workfunction.

The thickness of the lateral sidewall channel is a crucial design parameter that can have a significant impact on the performance of the DCVTFET. In Fig.11, the influence of varying channel thickness on the device performance is depicted. It is important to note that when the channel thickness is extremely thin, the quantum confinement effect leads to an increase in energy states within the channel. Consequently, a higher gate bias is required for tunneling to occur. Conversely, when the channel thickness is thick, the device performance deteriorates due to reduced gate controllability over the channel. The average subthreshold swing for channel thicknesses of 3nm, 5nm, and 10nm is measured to be 11.5, 20, and 39.6 mV/dec, respectively. Therefore, optimizing the channel thickness is essential to achieve optimal performance while maintaining a higher level of gate controllability.

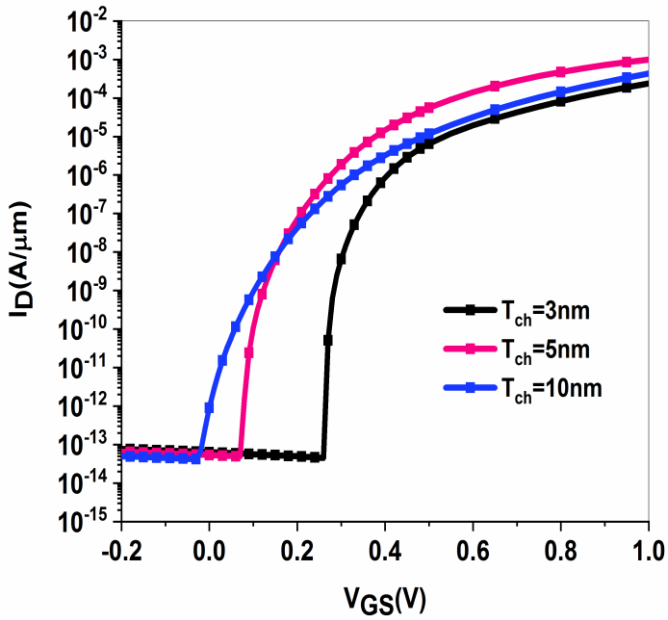

Fig.11: I_D-V_{GS} curves of DCVTFET as the lateral channel thickness is varied.

By definition, ambipolarity is recognized as a significant constraint of TFET device. Ambipolarity refers to the conduction of carriers in two directions, under both negative and positive gate bias. This phenomenon is primarily attributed to the movement of the tunneling junction from source to drain during n-TFET operation when the gate voltage is negative. The primary characteristic of the DCVTFET being suggested is the immunity of the tunneling junction to the drain electric field. As depicted in Fig. 12, even when the gate voltage is negatively biased, there is no presence of ambipolar current.

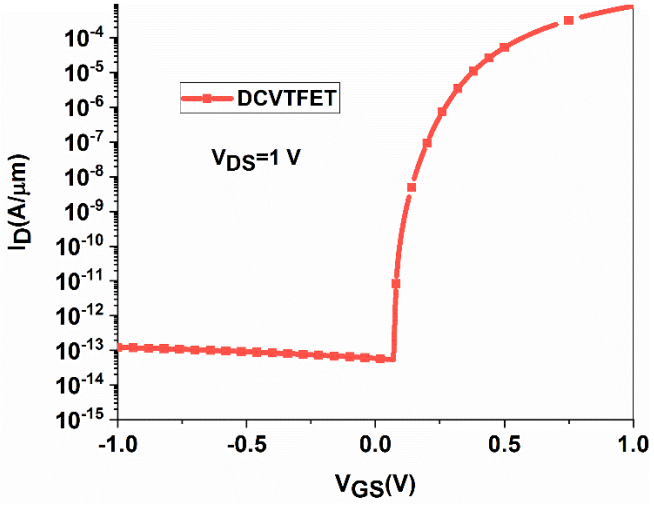

Fig. 12. I_D-V_{GS} curve of DCVTFET in the ambipolar state.

In order to accurately evaluate the sensitivity of the suggested electrical measures in relation to the fluctuation of crucial design parameters, a statistical analysis is conducted. This analysis involves calculating the percentile coefficient of variation for each electrical parameter. The coefficient of variation is defined as the ratio of the standard deviation to the mean value, and it serves as a valuable statistical measure that effectively demonstrates the degree to which the values in the dataset cluster around the mean value. The statistical analysis in Fig.13 demonstrates that the density of the source region is a crucial design parameter that can significantly impact the rate of tunneling and, consequently, the on-state current. However, when it comes to the off-state current, the device is not affected by variations in design parameters at room temperature, making it a suitable candidate for the nanoscale regime. Nevertheless, due to the extended source region, the off-state current is highly susceptible to temperature changes, primarily due to the increase in source minority carriers. The gate workfunction, on the other hand, is the most fundamental design parameter that influences the charge density in the channel. Therefore, the required bias for tunneling onset is highly dependent on the gate workfunction and must be optimized accordingly. A device with a low subthreshold swing is characterized by a rapid transition between the off (low current) and on (high current) states. At the room temperature, the thickness of the channel is the most critical design parameter that affects the subthreshold swing. The thickness of the side wall channels alters the controllability of the gate over the channel. In essence, a steep p^+-n^+ tunneling junction is necessary for tunneling onset, thus requiring a stronger electrostatic gate control to achieve a low subthreshold swing.

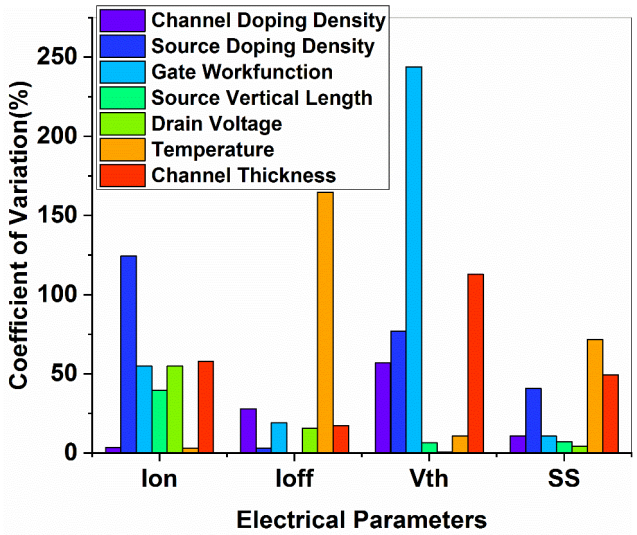

Fig. 13. Sensitivity of the DCVTFET electrical parameters with respect to the variation of critical design parameters. Sensitivity is defined as the coefficient of variation in percentile.

IV. CONCLUSION

This paper presents a novel approach to vertical TFET design by incorporating an extended source region and two side wall channels, resulting in enhanced tunneling rate. The impact of critical design parameters on device performance is thoroughly evaluated, and a statistical analysis is conducted to assess the sensitivity of the device electrical characteristics to variations in these parameters. The findings indicate that the DCVTFET device has successfully attained a considerably greater on-state drive current, surpassing the conventional TFET by a factor of 18, along with enhanced switching speed. The device's feasibility for high switching speed applications is attributed to its maximum subthreshold swing of 4.8 mV/dec. The findings highlight the significant role played by gate workfunction and source doping density in determining device performance, emphasizing the need to identify optimal values for these parameters. The data suggests that a workfunction of 5.3 eV is the optimal choice for the side wall gate in a heavily doped source region. Furthermore, the presence of an embedded oxide region between the source and drain regions provides high immunity to short channel effects, making this device a promising candidate for energy-efficient integrated circuits in the nanoscale regime.

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