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Impact of Oxide Thickness on the Electrical and Analog/RF Performance of Strained Heterojunction Gate-All-Around Nanosheet FETs

Reza Abbasnezhad [1]*

***Abstract*-- In this paper, the quantitative assessment of Heterojunction Gate All Around Nanosheet Field Effect Transistor (Heterojunction GAA NS FET) and Conventional Gate All Around Nanosheet Field Effect Transistor (Conventional GAA NS FET) performance was evaluated for different oxide thicknesses $t_{ox} = 0 \cdot 5.1 \cdot 0$ *and* $2 \cdot 0\ nm$). The effect of electrostatic control on DC and designing analog circuits, such as transconductance generation factor (TGF), Early voltage (V_{EA}), output conductance (g_d), transconductance (g_m), cut off frequency (f_T) have been investigated for all devices. Higher TGF and V_{EA} was achieved with $V_{GS} = 0 \cdot 22v$ for all devices. In the proposed Heterojunction GAA NS FET, we have used Germanium for the source region, Silicon/Germanium/Silicon (Si/Ge/Si) for the channel, and Silicon as the drain region. Incorporating strain in nanosheet and heterojunction structure devices can significantly improve device performance. Before using a model to analyz a semiconductor device, the model parameters must be accurately determined and elaborated. In this case, the Density Gradient (DG) equation, for a given electron Fermi-level distribution, has been solved self-consistently for the electrostatic potential, the Shockley-Read-Hall (SRH) equation for estimating carrier generation, bandgap narrowing for transport behavior and auger recombination. The general results show an improvement of approximately 10% in drain current, transconductance, and unity-gain frequency, providing superior RF performance of the heterojunction structure compared to the conventional GAA NS FET.**

***Index Terms*- Nanosheet, Heterojunction GAA NS FET, Conventional GAA NS FET, Density Gradient, On-Off-state.**

NOMENCLATURE

GAA NS FET (Gate All Around Nanosheet Field Effect Transistor).

I. INTRODUCTION

THE continuous scaling down of dimensions and weak electrostatic control in traditional planar bulk MOSFETs have led to short-channel effects and other undesirable properties. To address these challenges, the semiconductor industry must adopt novel device concepts that incorporate alternative mechanisms, non-planar structures, or innovative architectures [1]. The development of new architectures and devices is essential to mitigate adverse effects and improve channel control [2-4]. In line with Moore's Law, various technologies have been proposed to accommodate scaling limitations and new design layouts [5]. Since the introduction of MOSFETs, their dimensions have been progressively reduced, exacerbating short-channel effects (SCEs). However, modifications to fundamental structures provide viable solutions for achieving high-density chip integration [6].

Short-channel-enabled quantum effects play a crucial role in determining the transport characteristics of a system. Consequently, a detailed quantum-mechanical treatment of field-effect transistors (FETs) has become increasingly important in scaling theory to guide transistor development. As researchers continue to scale down FETs, they anticipate that

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1. Department of Electrical Engineering, Shabestar Branch, Islamic Azad University, Shabestar, Iran.
*Corresponding author Email: reza66.abbasnezhad@gmail.com

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reducing the channel length in modified-gate devices will enhance switching speed while also improving power handling and linearity [7]. According to the International Technology Roadmap for Semiconductors (ITRS), scaling complementary metal-oxide-semiconductor (CMOS) devices and integrated circuits (ICs) into the sub-nanometer regime necessitates advanced channel engineering techniques to mitigate gate leakage current and the worsening short-channel effects (SCEs) caused by continuous device miniaturization [8]. In recent decades, there has been a growing demand for the development of new devices capable of minimizing SCEs while maintaining optimal performance.

Researchers in the semiconductor industry have been exploring innovative device architectures, including double-gate [9], gate-all-around (GAA) [10], quadruple-gate [11], dual-material double-gate [12], triple-material double-gate [10], and nanosheet FETs [13], among others. Additionally, advancements in electrostatic control and the mitigation of short-channel effects (SCEs) have led to improvements in parameters such as parasitic capacitance, the I_{ON}/I_{OFF} ratio [14], and leakage current performance. One of the primary limitations of FETs in short-channel operation is the reduction in drive current due to the decreasing effective channel width as device dimensions are scaled down [15]. Due to poor electrostatic gate controllability and severe parasitic effects, GAA FETs have emerged as a promising alternative for sub-10 nm integrated circuit (IC) and CMOS technologies, potentially replacing FinFETs [16-17]. GAA FETs have garnered significant attention as the leading candidates for transistor scaling beyond FinFET technology [18]. Their multi-gate structure enhances gate control over the channel, effectively reducing SCEs and minimizing leakage currents. In our study, 3D stacking technologies were integrated with FinFET and multi-gate structures [19]. Nanosheet FET technology represents the most advanced node in semiconductor manufacturing for commercial logic devices, primarily due to its larger effective channel width and superior gate controllability compared to previous FET technologies. As researchers strive to balance device footprint with modern FET technology, key advancements are required to enhance device performance and gate controllability. In this context, heterojunction GAA nanosheet FETs have been investigated as potential candidates for future logic devices [20-21].

Recent innovations in semiconductor technology have introduced strain engineering and novel materials into IC and CMOS processes. These advancements include the incorporation of high-k dielectrics, metal-gate electrodes with tailored work functions, and the utilization of graphene nanomeshes in transistor channels [21], among others. As a result of these material innovations, new transistor architectures have emerged, with the heterojunction gate-all-around (GAA) nanosheet (NS) FET being a notable example. To enhance performance and power handling, these devices are designed in a stacked configuration, with series devices arranged in parallel. The heterojunction GAA NS FET represents a promising high-performance architecture for future semiconductor technologies, offering improved short-channel effects (SCEs) while requiring minimal modifications to FinFET integration. Further performance enhancements are expected through strategic manipulation of channel strain [22], as lattice strain serves as an effective approach for achieving equilibrium band structures [23-24].

While an experimental study of nanosheet transistors would provide more compelling validation, nanoscale devices with a gate length of $2 \cdot 0\, nm$, particularly those exploring digital, analog, and RF effects, are not yet widely available for direct comparison. Therefore, various similar structures will be proposed for evaluation. Previous studies have highlighted that heterojunction FETs utilizing germanium as the source material exhibit enhanced electrical performance [25-26]. The fabrication process of GAA-NSFETs has been documented in [27-28], where silicon sheets of varying thicknesses or SiGe were epitaxially grown within the channels. Experimental studies by Zhang et al. [29] and Sun et al. [30] have verified both the fabrication process and the improved electrical performance of gate-all-around silicon nanosheet devices. However, the influence of alternative source or drain materials, oxide thickness variations, and the impact of digital and analog/RF parameters at a 2 nm gate length have been less frequently explored in NSFET research. In this study, strain caused by lattice mismatch is considered a key factor contributing to carrier mobility enhancement. To further investigate this effect, a heterojunction structure and strain engineering have been integrated into a heterojunction GAA NS FET device using a multilayered Si/Ge/Si configuration. The remainder of this paper is organized as follows: Section 2 describes the design and geometry of the proposed NHJS and NCS devices, along with the simulation methodology. The potential applications of the proposed device are briefly introduced. Section 3 examines the impact of strain engineering and heterojunction structures on the electrical characteristics of the devices. Finally, Section 4 presents a summary of the key findings.

II. Device structure and Simulation method

A schematic representation of the 3D structure of both the proposed Heterojunction GAA NS FET and the Conventional GAA NS FET with a rectangular cross-section is shown in Fig. 1. As illustrated in Fig. 1, the proposed Heterojunction GAA NS FET features germanium as the source region, a silicon/germanium/silicon (Si/Ge/Si) channel, and silicon as the drain region [31]. In contrast, the Conventional GAA NS FET utilizes silicon for the source, drain, and channel regions. Among the various structures proposed to meet performance requirements [32], relaxed silicon was selected for the drain regions in both designs, while relaxed germanium was chosen as the source material for the Heterojunction GAA NS FET. Additionally, a strained-SiGe channel was employed, as tensile strain in SiGe induces a transformation in energy levels, thereby enhancing carrier transport properties [33]. The parameters used for the Heterojunction GAA NS FET and Conventional GAA NS FET in our simulations are summarized in Table I. In this context, t_{si} represents the silicon body thickness, *W* denotes the channel width, and L refers to the channel length. The metal gate work function is assumed to be 4.7 eV, with a gate oxide thickness ranging from 0.5 to 2 nm. Additionally, the material properties utilized in the simulations are summarized in Table II.

In the nanometer regime, the wave-like behavior of electrons becomes significant and must be considered in relation to the physical characteristics of quantum confinement and tunneling [35]. Various approaches are available for studying quantum transport. The confinement effects of electrons and holes, which are influenced by local potential variations on the scale of electron wave functions (i.e., quantum effects), can be modeled in Atlas using density-gradient theory. Density gradient theory is fundamentally equivalent to the Drift-Diffusion (DD) model in describing a semiconductor as comprising three components: an electron gas, a hole gas, and a rigid lattice continuum [36]. To enhance the accuracy of the Drift-Diffusion (DD) equations in semiconductor structures, various quantum corrections have been meticulously incorporated.

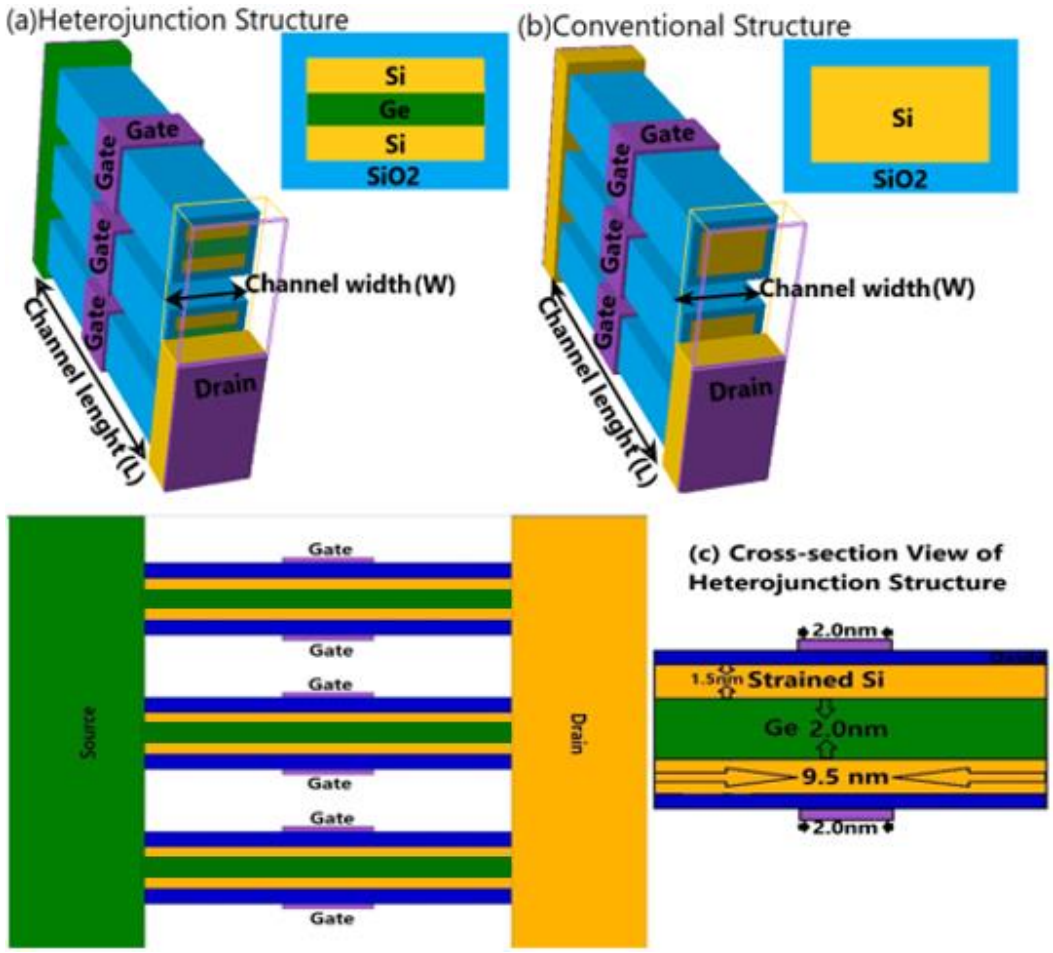

Fig. 1: Schematic view of the 3D of the (a) Heterojunction GAA NS FET and (b) Conventional GAA NS FET (c) Cross-section of view Heterojunction GAA NS FET

TABLE I
Parameters Used for Devices Modeled in this Work

Parameters	Heterojunction GAA NS WS FET	Conventional GAA NS FET
Channel material/hight(H)	Si/Ge/Si	Si
Gate length(L)	2.0nm	2.0nm
Source/Channel/Drain(L)	3nm/9.5nm/3nm	3nm/9.5nm/3nm
Channel width (W)	7nm/8nm/9nm	7nm/8nm/9nm
Gate Oxide Thickness	0.5nm/1.0nm/2.0nm	0.5nm/1.0nm/2.0nm
Source Material/doping	Relaxed-Ge/1*10^{13}cm^{-3}	Relaxed-Si/1*10^{13}cm^{-3}
Drain Material/Doping	Relaxed-Si /1*10^{13}cm^{-3}	Relaxed-Si/1*10^{13}cm^{-3}
Content of Ge in $Si_{1-x}Ge_x$	X = 0.2	-
Ge Layer diameter below the channel	2.0 nm	-

TABLE II
Material Properties Used in this Work (x is the Ge content in the $Si_{1-x}Ge_x$)[34]

Parametrs	Equation used
Electron affinity	$X_{Strained-Si} = 4 \cdot 05 + 0 \cdot 58x$ $X_{SiGe} = 4 \cdot 05 - 0 \cdot 05x$
Band gap energy	$E_{gStrained-Si} = 1 \cdot 12 - x(0.31 + 0.53x)$ $E_{gSiGe} = 1 \cdot 12 - 0 \cdot 42x$
Conduction band offset	$\Delta E_c = 0 \cdot 63x$
Valance band offset	$\Delta E_v = x(0 \cdot 74 - 0 \cdot 53x)$

The Density Gradient (DG) model can be regarded as a direct extension of the DD theory, providing improved accuracy in capturing quantum effects [37]. In many semiconductor devices, quantum mechanical phenomena such as evanescent wave effects occur within "quantum wells," where (quasi) equilibrium is established by confining potential barriers in one-, two-, or three-dimensional structures [38].

In our simulations, it is assumed that the inversion and accumulation layers follow the behavior of an electron gas, causing their properties to change rapidly near the interface. To account for quantum confinement effects, Density Gradient (DG) quantum corrections for carriers have been implemented in the simulator.

Typically, in the solution of the density gradient (DG) corrected drift diffusion (DD) approximation, we use a modified Gummel approach [39], where the Poisson equation (1) and density gradient (DG) equation (2), for a given electron Fermi-level distribution, are solved self-consistently for the electrostatic potential and the quantum-corrected electron density:

$$\nabla \cdot (\varepsilon \nabla \psi) = -q(p - n + N_D^+ - N_A^-) \quad (1)$$

where ψ is the electrostatic potential, ε is the dielectric constant of the material, q is the electronic charge, p is the hole concentration, n is the electron concentration, N_D is the donor concentration and N_A is the acceptor concentration. Also in (2). Equation (2) is the anisotropic density gradient equation, so there are different effective mass components in the transport (longitudinal) direction from in the confinement (transverse) direction.

$$\frac{2b_n^*}{S}\left(\frac{1}{m_x}\frac{\partial^2 S}{\partial x^2} + \frac{1}{m_y}\frac{\partial^2 S}{\partial y^2} + \frac{1}{m_z}\frac{\partial^2 S}{\partial z^2}\right) = \emptyset_n - \psi + \frac{K_B T}{q}\ln(S^2) \quad (2)$$

Where $S = \sqrt{n/n_i}$, $b_n^* = \hbar/4qr$, $\emptyset_n$ is the quasi-Fermi level, ψ is the electrostatic potential, ε is the local permittivity, K_B is the Boltzmann constant, T is lattice temperature and m is the carrier effective mass. The effective quantum-corrected potential is then calculated from (3) as follows [40]:

$$\psi_{eff} = \psi + \frac{2b_n^+}{S}\left(\frac{1}{m_x}\frac{\partial^2 S}{\partial x^2} + \frac{1}{m_y}\frac{\partial^2 s}{\partial y^2} + \frac{1}{m_z}\frac{\partial^2 S}{\partial z^2}\right) = \emptyset_n + \psi + \frac{K_B T}{q}\ln(S^2) \quad (3)$$

which is then used as the driving potential for the current continuity equation:

$$\nabla . J_n = 0 \quad (4)$$

Where

$$J_n = -qn\mu_n \nabla \psi_{eff} + qD_n \nabla_n \quad (5)$$

To improve efficiency, a Scharfetter-Gummel discretization scheme is implemented based on the effective quantum-corrected potential [41]. The system of equations is solved using the 3D ATLAS simulator. The bandgap narrowing (BGN) model is applied to accurately predict subthreshold behavior and Auger recombination [42-43], and these models are incorporated into the simulations. The Shockley-Read-Hall (SRH) model is used to estimate carrier generation and recombination mechanisms, providing insight into doping-induced device properties. Fermi-Dirac (F-D) statistics, which describe the probability of electron or hole occupation of a given energy level under equilibrium conditions, are also considered [44]. As illustrated in Fig. 2, the transfer characteristics of the main structure were compared with the transfer characteristics curve in reference [26] to calibrate the parameters and models used in the simulations.

The system of equations (1, 2, and 4) is solved self-consistently until convergence is reached. Dirichlet boundary conditions are applied at the interfaces between the source, channel, and drain contacts.

III. Results and Discussions

The drain current of the Heterojunction GAA NS FET and the Conventional GAA NS FET with different oxide thicknesses versus V_{GS} at V_{DS}=0.8V are shown in Fig. 2. The threshold voltage shift and drive current that both occur with the application of voltage have a considerable effect on the performance of the structures. The threshold voltage was extracted under a current of $1 \cdot 0\ nA$ at V_{DS}=$0 \cdot 8$V [45]. The threshold voltage of a device is a critical parameter for its performance. Any changes to the device structure, such as strain engineering or heterojunction integration, can either increase or decrease the threshold voltage. In the case of the Conventional GAA NS FET, the threshold voltage is lower compared to the Heterojunction GAA NS FET. The reduction in threshold voltage with varying oxide thicknesses ($t_{ox} = 0 \cdot 5.1 \cdot 0\ and\ 2 \cdot 0\ nm$) is approximately 7%, 9.5%, and 13.5%, respectively. A decrease in the electrical field confines fewer carriers near the surface, which in turn increases mobility and consequently lowers the threshold voltage.

The threshold voltages of the Heterojunction GAA NS FET and Conventional GAA NS FET with varying oxide thicknesses are summarized in Table III. Drive current is directly influenced by the device characteristics, such as the energy band structure

in both the on-state and off-state. The characteristic curve for the Heterojunction GAA NS FET shows the maximum current, indicating superior performance. Notably, the Heterojunction GAA NS FET exhibits higher drain current, which can be attributed to its enhanced mobility, higher drive currents, and better electrostatic performance compared to the Conventional GAA NS FET. Furthermore, the results and proposed mechanisms can be applied to a range of applications, including biosensors, non-volatile memory devices, and investigations into ageing effects [46].

The variations in drain current for both the Heterojunction GAA NS FET and Conventional GAA NS FET as a function of drain voltage are shown in Fig. 3 at $V_{GS} = 1.0\ v$. When a drain voltage is applied, charge carriers move through the channel region. As V_{DS} increases, more charge carriers attempt to pass through the narrow channel. However, beyond a certain value, the drain current saturates even with further increases in the drain voltage.

This saturation can be attributed to the strain engineering and heterojunction structure, which improve carrier transport efficiency in the Heterojunction GAA NS FET by directing more carriers toward the drain side. The drain current is notably higher for the Heterojunction GAA NS FET compared to its Conventional GAA NS FET counterpart, as shown in the characteristic curve. The electrical characteristics of both the Heterojunction GAA NS FET and the Conventional GAA NS FET are summarized in Table III. Additionally, the on-state and off-state currents for the presented structures are provided in Fig. 4.

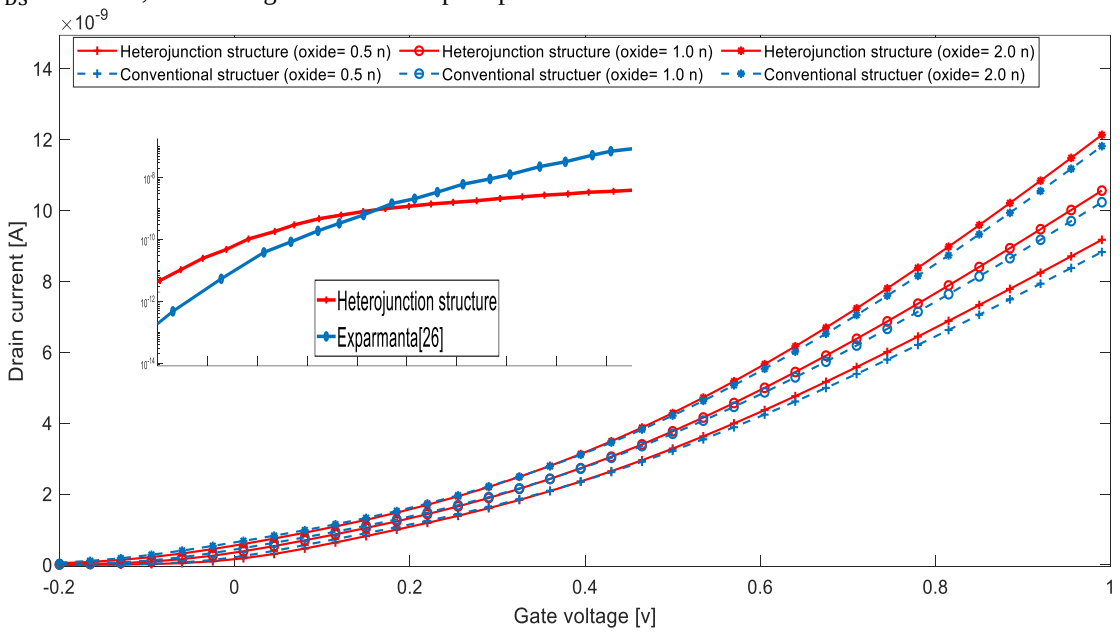

Fig. 2: Drain current of the Heterojunction GAA NS FET and the Conventional GAA NS FET versus at V_{DS}=0.8V

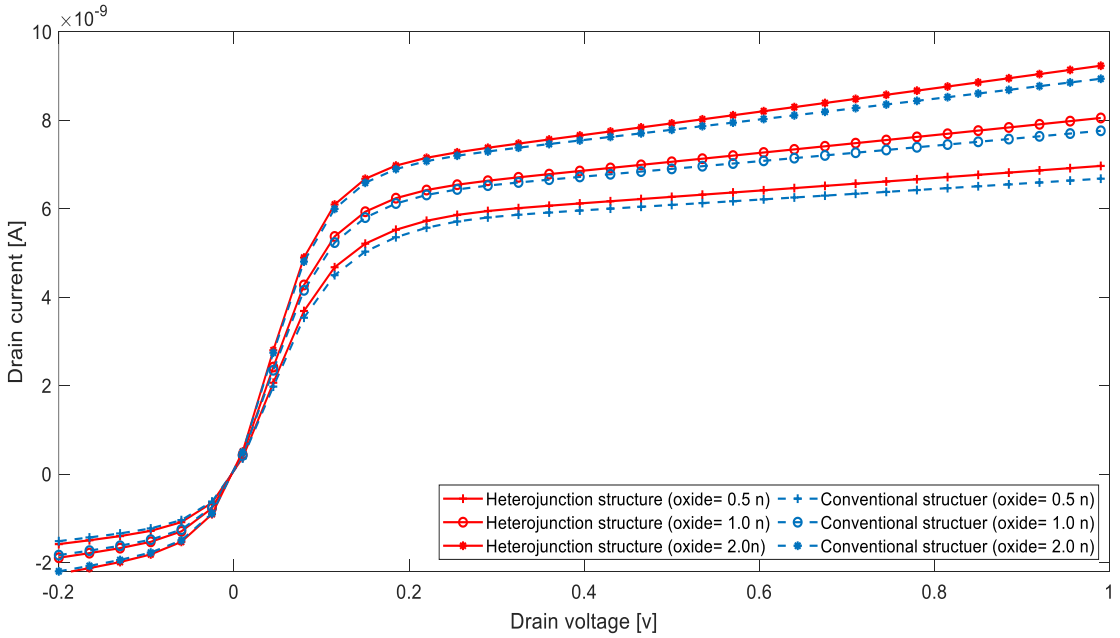

Fig. 3: Variation of drain current for Heterojunction GAA NS FET and Conventional GAA NS FET under various V_{DS} values at V_{DS}=0.8

TABLE III
Electrical Characteristics of Heterojunction GAA NS FET and Conventional GAA NS FET.

Parameters	Heterojunction GAA NS FET	Conventional GAA NS FET
$\mathbf{V_{th}(v)(oxide = 0 \cdot 5\ nm)}$	0·185	0·1713
$\mathbf{V_{th}(v)(oxide = 1 \cdot 0\ nm)}$	0·141	0·127
$\mathbf{V_{th}(v)(oxide = 2 \cdot 0\ nm)}$	0·0975	0·084
$\mathbf{DIBL(oxide = 0 \cdot 5\ nm)}$	0·418	0·426
$\mathbf{DIBL(oxide = 1 \cdot 0\ nm)}$	0·448	0·4501
$\mathbf{DIBL(oxide = 2 \cdot 0\ nm)}$	0·481	0·479
$\mathbf{I_{ON}/I_{OFF}\ (A)\ (oxide = 0 \cdot 5\ nm)}$	$4 \cdot 4328 + 10^{-3}$	$3 \cdot 2841 + 10^{-3}$
$\mathbf{I_{ON}/I_{OFF}(A)(oxide = 1 \cdot 0\ nm)}$	$8 \cdot 01 + 10^{-3}$	$5 \cdot 888 + 10^{-3}$
$\mathbf{I_{ON}/I_{OFF}(A)(oxide = 2 \cdot 0\ nm)}$	$2 \cdot 458 + 10^{-3}$	$1 \cdot 787 + 10^{-3}$

If the I_{ON}/I_{OFF} ratio is a critical parameter for IC and CMOS technologies, having a significant impact on low standby power applications. Heterojunction GAA NS FET devices offer greater space in the source-channel region for carriers to drift when the transistor is in the ON state. This enhanced drift velocity in the source and the effective channel width results in a higher ON current for the Heterojunction GAA NS FET. Furthermore, the conduction band offset energy increases the kinetic energy of electrons, leading to a higher I_{ON}. The combined effect of strain and heterojunction engineering also modifies the channel band structure, improving carrier confinement and further facilitating efficient electron transport across the channel. As a result, the Heterojunction GAA NS FET exhibits superior switching characteristics, with a higher I_{ON}/I_{OFF} ratio (approximately 30%) compared to the Conventional GAA NS FET.

The variation in electron densities with the same gate-to-source voltage but different oxide thicknesses for the Heterojunction GAA NS FET and Conventional GAA NS FET is shown in Fig. 5 (A to D). The figures illustrate the different stages of electron density for both devices. As shown, the channel begins to form at the upper and lower gates. In the Conventional GAA NS FET (Fig. 5 A-C), the electron density is low, and there are insufficient carriers in the channel region. In contrast, in Fig. 5 (B-D), the electron density increases from both the upper and lower gates, leading to channel formation. This increase in electron density is enhanced in the Heterojunction GAA NS FET due to the combined effects of strain and the heterojunction structure. Specifically, the lattice mismatch introduced by the SiGe layers in the channel generates mechanical strain, which modifies the silicon band structure and reduces the carrier effective mass. At the same time, the heterojunction creates a conduction band offset that confines carriers more effectively.

Together, these effects improve carrier accumulation and control in the channel, enabling higher electron densities and more efficient channel formation compared to the Conventional GAA NS FET.

The velocity can be calculated using the equation $I = qnva$ [47], where A is the cross-sectional area, q is the carrier charge, n represents the electron density (as shown in Fig. 6), and v is the electron velocity. As depicted in Fig. 6, the electron velocity is higher in the channel region of the Heterojunction GAA NS FET compared to the Conventional GAA NS FET. In the proposed Heterojunction device, electrons are injected into the channel with increased velocity due to the conduction band offset at the source-channel interface, which accelerates carriers and enhances transport efficiency. This mechanism contributes to improved current drive and overall device performance in the heterojunction structure.

Due to the strain and heterojunction structure, the Heterojunction GAA NS FET exhibits 67%, 70%, and 73% enhancements in electron velocity for different oxide thicknesses $(t_{ox} = 0 \cdot 5.1 \cdot 0\ and\ 2 \cdot 0\ nm)$ respectively, compared to the Conventional GAA NS FET.

In off-state mode, I_{OFF} is independent of the gate voltage, but increases with the increasing drain voltage as shown in Fig. 4. The comparative analysis of energy band diagrams in the S/D edge region for both Heterojunction GAA NS FET and Conventional GAA NS FET in the off-state is shown in Fig. 7(a). In the OFF-state, there are insufficient carriers in the source to be injected into the channel for both structures. To achieve high performance, it is essential to deplete the channel to attain an acceptably low off-state current. When a positive voltage is applied to the structure, the number of carriers transferred to the gate electrode increases, leading to accumulation in the layer beneath the gate. As the gate voltage increases, the energy bands of the channel shift, reaching the flat band region. For the ON-state current, the electron velocity and peak electron velocity near the source region provide additional acceleration to electrons in the channel. Enhanced carrier accumulation and velocity near the source region are illustrated in Fig. 7(b).

As the gate voltage gradually increases, the heterojunction structure near the extended-source channel region leads to more pronounced band bending, resulting in stronger electron velocity. The electron carriers are able to achieve a higher drift velocity, enabling them to overcome the barrier width and causing a sharp increase in the drain current. As shown in Fig. 7(b), the Heterojunction GAA NS FET device outperforms the Conventional GAA NS FET device. This performance enhancement can be attributed to the presence of the heterojunction and strain in the Si/Ge/Si channel region, which significantly improves carrier transport in the Heterojunction GAA NS FET compared to the Conventional GAA NS FET.

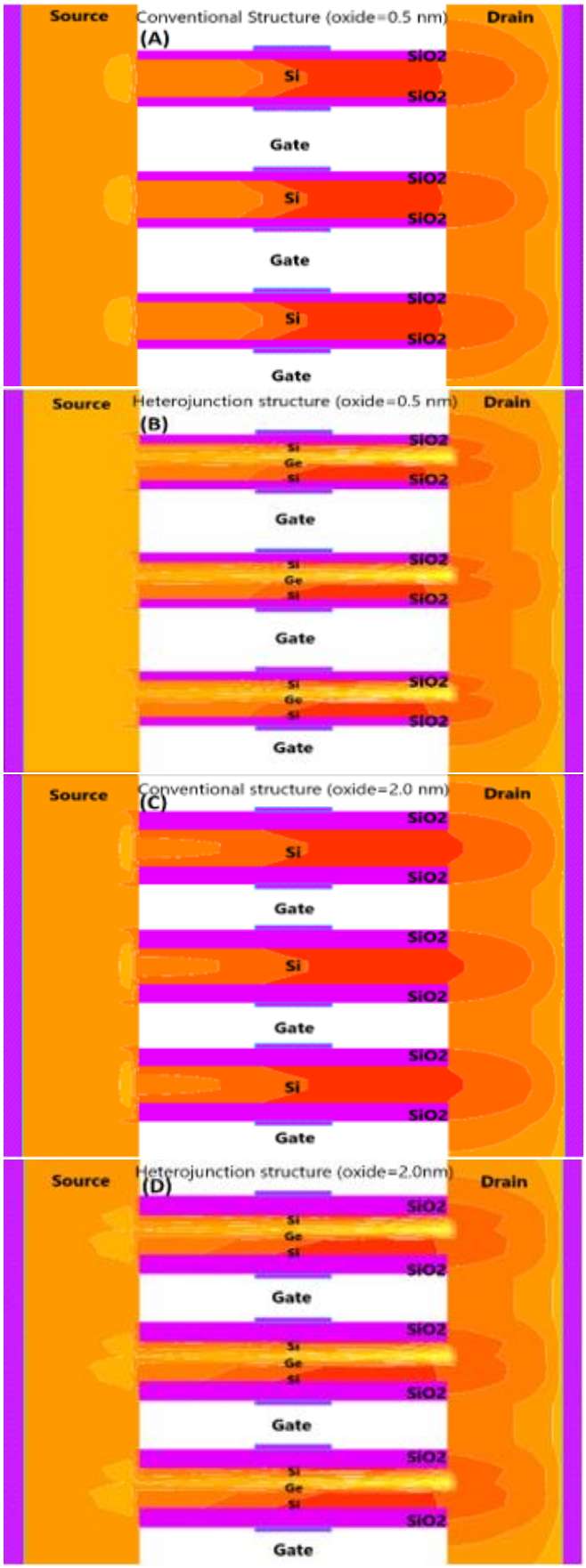

Fig. 5 (A-D): Electron densities varying with the same gate to source voltage for Heterojunction GAA NS FET and Conventional GAA NS FET with different oxides

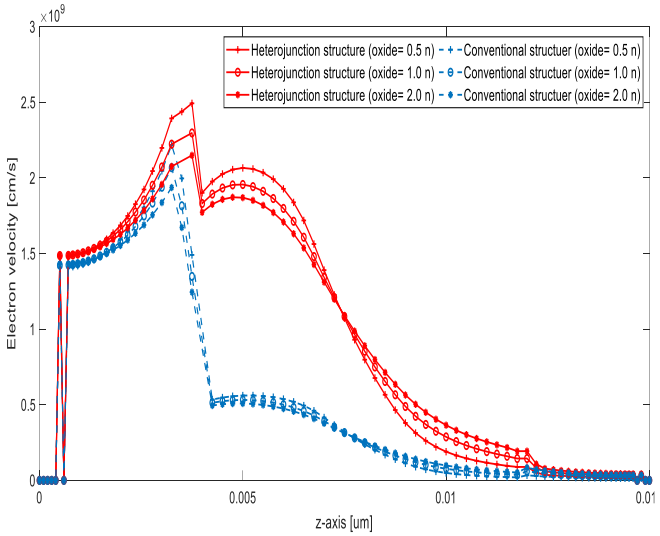

Fig. 6: Electron velocity in the horizontal direction in the S/D edge region for both Heterojunction GAA NS FET and Conventional GAA NS FET

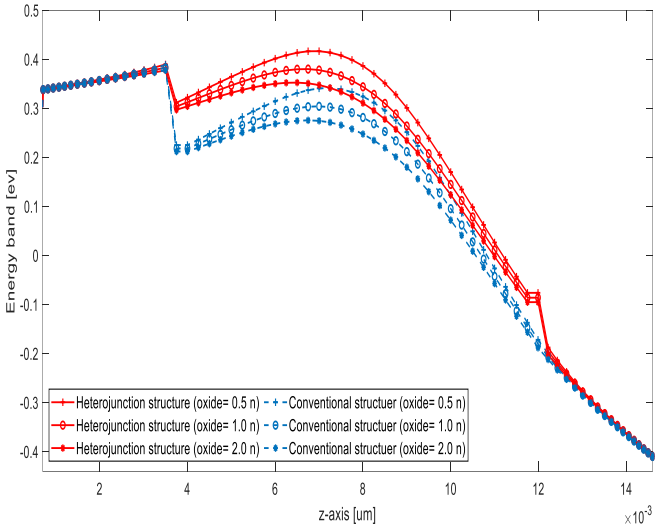

Fig. 7(a): Band diagram in the horizontal direction in the S/D edge region for both Heterojunction GAA NS FET and Conventional GAA NS FET in the off-state.

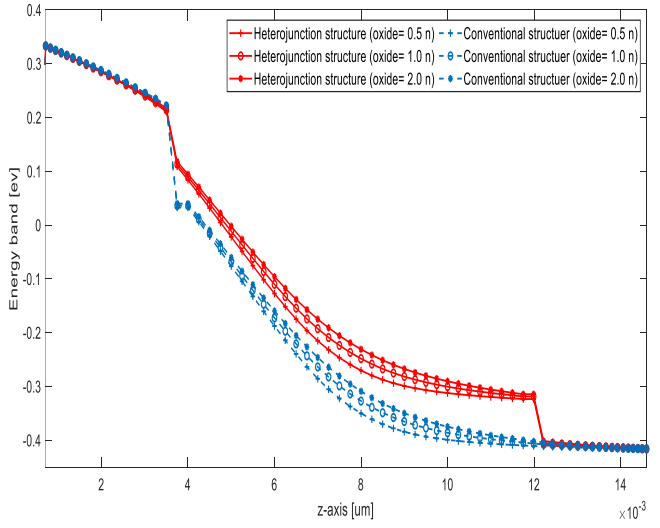

Fig. 7(b): Band diagram in the horizontal direction in the S/D edge region for both Heterojunction GAA NS FET and Conventional GAA NS FET in the on-state.

In addition to the electrical characteristics of the devices, other important parameters for analog/RF circuits must be considered. When designing analog circuits, key parameters include transconductance (g_m), the transconductance generation factor (TGF), output conductance (g_d), total gate capacitance (C_{GG}), and the cut-off frequency. To achieve a certain transconductance value, the TGF can be utilized. The key analog parameters for this technology are V_{EA} and TGF, which demonstrate the efficiency of the devices in converting DC power into AC frequency. V_{EA} and TGF has been calculated as $TGF = g_m/I_d$ and $V_{Early} = I_D/g_d$.

The high TGF ratio contributes to superior performance in circuits operating at low supply voltages. For the computation of TGF and V_{EA}, a constant $V_{DS} = 0 \cdot 8$ v is maintained. By analyzing the equations for V_{EA} and TGF, it can be observed that, due to the higher transconductance (Fig. 8), both V_{EA} and TGF are greater for Heterojunction GAA NS FET devices. The output conductance (g_d) as a function of V_{DS} for different cases at $V_{GS} = 1 \cdot 0$ v is defined and calculated as $g_d = \partial I_D/\partial V_{DS}$. The increase in the width of the drain depletion region in Heterojunction GAA NS FET devices results in higher output conductance compared to Conventional GAA NS FET devices.

The concept of high g_d is associated with an increase in I_D with V_{DS} in the saturation regime. Conversely, a low g_d corresponds to a higher Early voltage. Enhancing g_d reduces the output resistance.

Since the Heterojunction GAA NS FET enters the saturation region earlier, a higher g_d can be achieved. Upon analyzing the results, it was observed that the Heterojunction GAA NS FET devices exhibit approximately 8% higher efficiency in g_d compared to the Conventional GAA NS FET devices. All the extracted values for optimal performance conditions of the analog/RF parameters are summarized in Table IV.

TABLE IV
Extracted Values for Analog/RF Parameters of Heterojunction GAA NS FET and Conventional GAA NS FET

Paramaeters	Heterojunction GAA NS WS FET	Conventional GAA NS FET
TGF(oxide = 0 · 5 nm)	18.8	18.2
TGF(oxide = 1 · 0 nm)	12.12	10.75
TGF(oxide = 2 · 0 nm)	8.485	7.236
g_d(oxide = 0 · 5 nm)	6.8e-8	6.15e-8
g_d(oxide = 1 · 0 nm)	5.487e-8	5.333 e-8
g_d(oxide = 2 · 0 nm)	4.81e-8	4.507e-8
V_{EA}(oxide = 0 · 5 nm)	1.2	1.093
V_{EA}(oxide = 1 · 0 nm)	1.477	1.389
V_{EA}(oxide = 2 · 0 nm)	1.675	1.61

Transconductance (g_m) is a crucial factor in increasing the speed of a circuit and is calculated as $g_m = \partial I_{DS}/\partial V_{GS}$. The transconductance characteristics of the strained heterojunction GAA NS FET and the Conventional GAA NS FET at $V_{DS} = 0 \cdot 8v$ V are shown in Fig. 8. A higher g_m indicates greater channel transport efficiency, higher voltage gain, and better suitability for analog applications, enabling faster device operation. As shown in Fig. 8, the transconductance of the strained heterojunction device is significantly higher than that of the conventional structure. This improvement is primarily due to the combined effects of strain engineering and the heterojunction channel design: the lattice-mismatch-induced strain reduces the carrier effective mass and increases mobility, while the heterojunction creates a conduction band offset that confines carriers and enhances their injection from the source. Together, these mechanisms reduce channel resistance, improve current conduction through the source-channel junction, and increase electron velocity, ultimately boosting g_m and the overall analog performance of the device. Additionally, for fast switching below the threshold, a smaller g_m can still be effectively utilized without compromising switching speed.

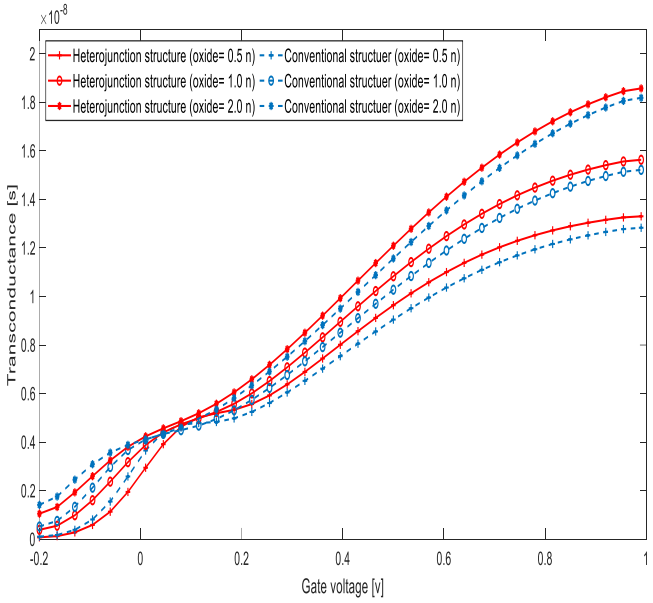

Fig. 8: Transconductance (gm) characteristics of the Heterojunction GAA NS FET and Conventional GAA NS FET at V_{DS} =0.8V.

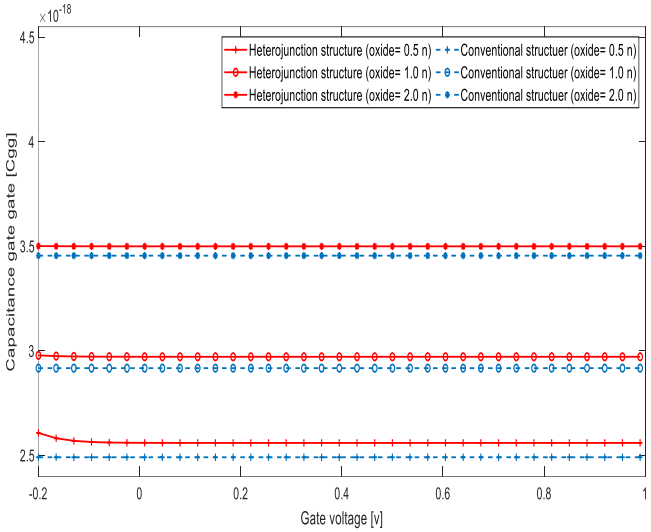

Fig. 9: The total gate capacitance is an important parameter for the high-frequency performance analysis.

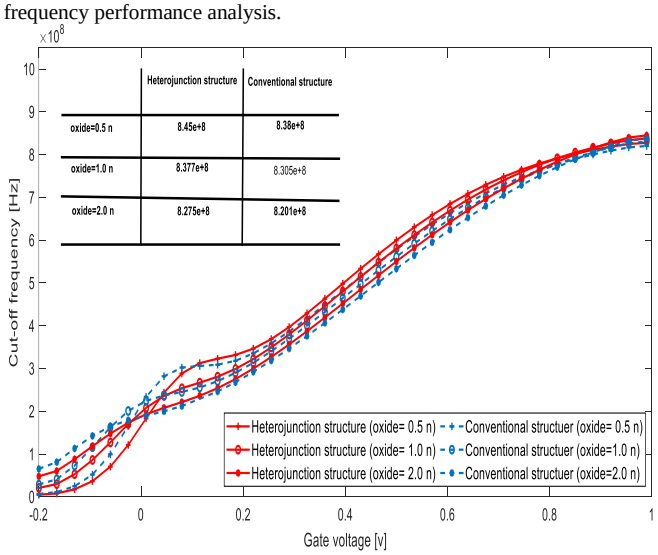

Fig. 10: Cut-off frequency characteristics of the Heterojunction GAA NS FET and Conventional GAA NS FET

The variation in total gate capacitance (C_{GG}) as a function of V_{GS} is plotted in Fig. 9. The performance of MOSFET devices depends on the total gate capacitance, which can be improved by reducing the C_{GG} value. In both Heterojunction GAA NS FET and Conventional GAA NS FET structures, capacitance increases with V_{GS}, leading to higher delay times and, consequently, lower switching speeds. However, strain in the channel and the heterojunction at the source region result in higher capacitance due to the increased area of parasitic capacitance. As shown in Fig. 9, switching speed can be controlled by varying the oxide thickness. When the oxide thickness increases from 0.5 nm to 2 nm, C_{GG} is observed to decrease. It is evident that the gate capacitance value for the Heterojunction GAA NS FET is higher than that of the Conventional GAA NS FET for all applied gate-source voltages.

The cut-off frequency (F_T) of the device depends on both the transconductance (g_m) and the total gate capacitance (C_{GG}). The cut-off frequency characteristics of the Heterojunction GAA NS FET and Conventional GAA NS FET are shown in Fig. 10. The cut-off frequency is calculated from $F_T = (g_m/2\pi C_{GG})$. The peak value of F_T is higher for the Heterojunction GAA NS FET due to better gate control and increased transconductance. The cut-off frequencies for both Heterojunction GAA NS FET and Conventional GAA NS FET are summarized in Fig. 10.

IV. Conclusion

The different device performance parameters of operation were systematically investigated for the heterojunction GAA NS FET and conventional GAA NS FET devices. The results showed that, within the scope of the density gradient model, the Heterojunction GAA NS FET structure achieved high on-state current and low off-state current. In addition, investigated analog/RF parameters such as V_{EA}, TGF, g_d and F_T for two different device configurations with different oxide thicknesses. The I_{ON}/I_{OFF} ratio, for Heterojunction GAA WS FET and Conventional GAA NS FET with different thicknesses ($t_{ox} = 0 \cdot 5.1 \cdot 0\ and\ 2 \cdot 0\ nm$) are 39%, 36%, and 33.7%, respectively, which shows improvement in heterojunction structures. On the other hand, the heterojunction GAA NS FET device, i.e. ($t_{ox} = 2 \cdot 0nm$), shows an improvement in TGF, V_{EA} and g_d ratios of 17.2%, 4%, and 6.72%, respectively, over its counterparts. Despite the large capacitance, due to the admissible transconductance, the cut-off frequency (F_T) in the heterojunction GAA NS FET was higher than that of the conventional GAA NS FET. Improvements in these electrical parameters have been obtained, and the Heterojunction GAA NS FET offers preferable electrical characteristics over the conventional structure, because increased performance provides significant improvement.

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Conflicts of Interest

The author declares no conflict of interest.

Authors' Contributions

The author confirms sole responsibility for the following: study conception and design, data collection, analysis and interpretation of results, and manuscript preparation.

Statement on the use of Generative AI

The author declares that no generative AI tools were used in the preparation of this manuscript.

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