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Modeling of the LDMOSFET Transistor with P-Type Windows Based on the BSIM6 Model

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***Abstract*-- A physics-based circuit model is presented for a P+ window lateral double-diffused MOSFET (PW-LDMOSFET) structure intended for high-voltage circuit applications. The device employs p-type windows underneath the drift region to reshape the electric field to improve the breakdown voltage. In the proposed model, the PW-LDMOSFET structure is partitioned into two main parts: First, an intrinsic MOSFET modeled by the BSIM6 compact model and second, a voltage-controlled resistor network that represents the segmented drift region. The drift region is divided into six regions, and closed-form analytical expressions are derived for each segment, explicitly accounting for the influence of the depletion effect of P-N junctions on the effective conduction thickness. To verify the proposed model, the PW-LDMOSFET structure is simulated and analyzed using the SILVACO-ATLAS two-dimensional device simulator, including several physical models, and the results are then compared with the proposed model implemented in SILVACO-SmartSpice. Comparisons between the results demonstrate accurate prediction of the drain current characteristics and the dependence of on-resistance on gate voltage and doping concentration of the drift region for gate biases above threshold. Due to the modular formulation of the proposed model, it can be extended to other LDMOSFET structures that use p-type windows.**

***Index Terms*- BSIM6, Circuit Model, LDMOSFET, On-Resistance, SILVACO, Voltage-Controlled Resistor (VCR).**

I. INTRODUCTION

LATERAL double-diffused metal-oxide-semiconductor field-effect transistors (LDMOSFETs) are widely used in high-voltage integrated circuits as amplifiers, rectifiers, switches, and in satellite/military applications [1–3]. Accurate current-voltage (I-V) modeling is essential due to its diverse applications, prompting extensive research [4–7]. Typically, LDMOSFETs are modeled with an intrinsic channel as a standard MOSFET and the drift region as a voltage-controlled resistor [4,6–11].

In recent years, a variety of novel device structures have been proposed to enhance the key figures of merit of LDMOSFETs such as on-resistance (R_{on}) and breakdown voltage (BV) [12–16]. One widely investigated approach in these structures is the RESURF technique. In RESURF-based designs, the depletion region extends across the drift region, resulting in a more uniform redistribution of the electric field. This electric-field shaping increases the breakdown voltage and enables higher drift-region doping, thereby reducing the on-resistance. [17–20].

Owing to the structural modifications introduced in LDMOSFET transistors, this study aims to develop a modeling approach for novel LDMOSFET structures that employ p-type windows underneath the drift region. The device structure presented in [21], referred to as P^+ window LDMOS (PW-LDMOSFET), is selected as the base structure for the proposed modeling framework.

In this work, the LDMOSFET is modeled using the BSIM6 MOS model for the intrinsic channel in conjunction with a modified voltage-controlled resistor to represent the drift region. BSIM6 is the most recent compact model for bulk MOSFETs developed by the BSIM group and features a body-referenced, charge-based core formulation [22].

Furthermore, the SILVACO-ATLAS two-dimensional (2D) device simulator is employed to simulate the PW-LDMOSFET structure and to validate the proposed model [23]. In the subsequent section, the PW-LDMOSFET structure is described in detail, and the method for extracting the resistance associated with the drift region is presented. Finally, the results of the proposed model are compared with

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those of the PW-LDMOSFET structure to assess the accuracy and reliability of the developed modeling approach.

II. PW-LDMOSFET Structure and Modeling

A. PW-LDMOSFET Structure

In this paper, the PW-LDMOSFET structure proposed in [21] is adopted as the baseline device. This structure achieves a breakdown voltage of 405 V, as reported in [21]. Fig. 1 illustrates the schematic of the PW-LDMOSFET. The key feature of the PW-LDMOSFET is the incorporation of p-type windows beneath the drift region. The implantation of these p-type windows modifies the electric-field distribution within the drift region, leading to the formation of additional electric-field peaks. The resulting electric-field distribution, as reported in [21], is shown in Fig. 2.

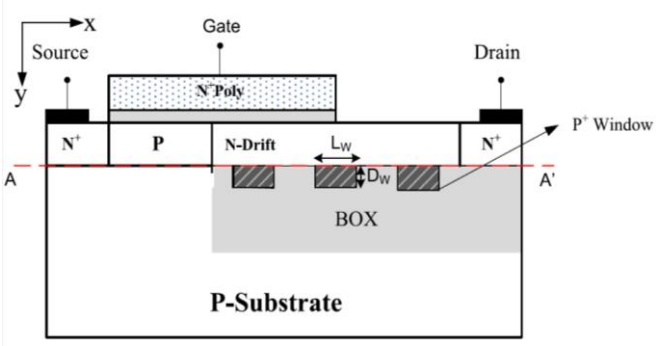

Fig. 1. Overview of the PW-LDMOSFET structure [21].

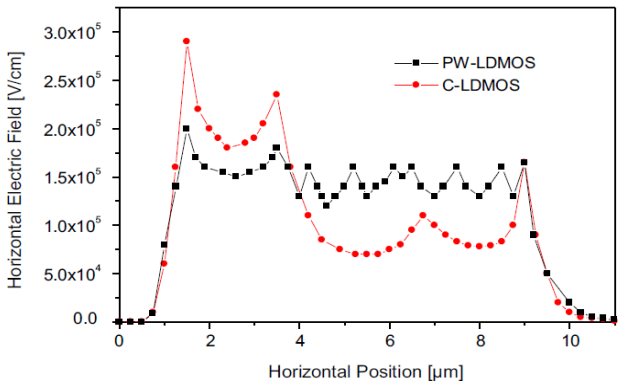

Fig. 2. Horizontal electric field distribution of PW-LDMOSFET compared to conventional (Along Cutline AA') [21].

B. Modeling

For modeling, the PW-LDMOSFET structure is divided into two main components. The first component is a conventional MOSFET, while the second component consists of voltage-controlled resistive elements. The transistor component is modeled using the BSIM6 model implemented in the SILVACO SmartSpice simulator [22,24]. The voltage-controlled resistance represents the total resistance of the PW-LDMOSFET drift region.

To calculate the voltage-controlled resistance, the drift region is divided into multiple sections. As shown in Fig. 3, the segmentation of the drift region is based on the spatial positions of the depletion regions within this area. In the PW-LDMOSFET, the depletion region of the p-window adjacent to the channel overlaps with the depletion region of the channel–drift P–N junction; therefore, these two regions are treated as a single combined region. Therefore, the drift region of the PW-LDMOSFET is divided into six sections. Accordingly, the total resistance of the drift region, as expressed in (1), is obtained by summing the resistances of these sections. Fig. 4 presents the equivalent circuit model of the PW-LDMOSFET.

$$R_{Total-Drift} = R_1 + R_2 + R_3 + R_4 + R_5 + R_6 \quad (1)$$

As shown in Fig. 3, R_1 represents the resistance of region 1 adjacent to the channel and the p-type window. The resistances of the regions l between the two p-type windows are represented by R_2 and R_4. The resistance of the region between the p-type window and the drain is denoted as R_6. The resistance R_3 represents region 3, which includes both gate-overlapped and non-overlapped portions of the device. To simplify the analysis and improve the accuracy of the proposed model, several assumptions are adopted, as explained below.

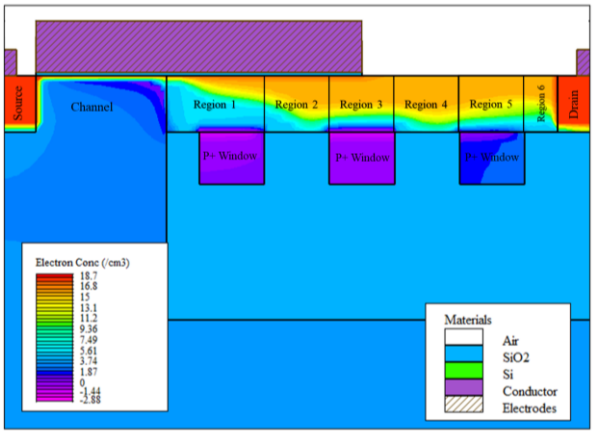

Fig. 3. Electron concentration in PW-LDMOSFET at $V_{GS} = 5V$ and $V_{DS} = 10\,V$

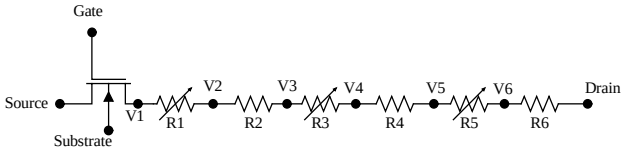

Fig. 4. Circuit model of PW-LDMOSFET with the drift region resistors.

The resistance of each region is calculated using

$$R = \rho \frac{L}{A} \quad (2)$$

where R is the resistance of the region, ρ is the resistivity (dependent on doping concentration and material type), L is the region length, and A is the active area for current flow.

The active area A is expressed as the product of the region thickness and width. While the thickness varies among regions, the width remains constant and is equal to the device width, denoted by W. Accordingly, (2) can be rewritten as (3).

$$R = R_{sh} \frac{L}{T} \quad (3)$$

Here, $R_{sh} = \frac{\rho}{W}$ is the sheet resistance and T denotes the thickness of each region. Based on these relations and the initial modeling assumptions, the resistance of each region is determined.

1) Resistance of region 1(R_1)

To calculate the resistance of region 1, the equations presented in [25] are employed. The total resistance of region 1, without considering the depletion region, is denoted as $R_{1-general}$. As illustrated in Fig. 5, region 1 is modeled as

two components, R_{1-dep} and R_1. Based on (4), as explained in [25], $R_{1-general}$ is obtained as the parallel combination of R_{1-dep} and R_1.

$$R_{1-general} = R_1 \| R_{1-dep} \quad (4)$$

Here, R_{1-dep} represents the resistance associated with the depletion region, while R_1 corresponds to the actual conductive resistance of region 1 in the current path. Considering this, R_1 can be calculated as:

$$R_1 = \frac{R_{1-general}}{1 - \frac{R_{1-general}}{R_{1-dep}}} \quad (5)$$

Based on the equations presented in [25], the resistances $R_{1-general}$ and R_{1-dep} are calculated using (6) and (7), respectively:

$$R_{1-general} \cong \frac{2}{\pi} R_{sh} \ln \frac{L_1}{r_1} \quad (6)$$

$$R_{1-dep} \cong \frac{3}{2} R_{sh} \frac{L_1 - r_1}{\sqrt{\frac{2\varepsilon_{si}}{q} \times \frac{N_{ch}}{N_{dr}(N_{ch} + N_{dr})}(V_2 - V_1)}} \quad (7)$$

Here, ε_{si} is the silicon permittivity coefficient, N_{dr} and N_{ch} denote the doping concentrations of the drift region and the transistor channel, respectively, while L_1 represents the length of region 1. Based on the PW-LDMOSFET structure, r_1 is obtained as:

$$r_1 = \sqrt{\frac{2\varepsilon_{si}(V_{gs} - \phi_{ms})}{qN_{ch}}} \quad (8)$$

Here, V_{gs} denotes the gate-to-source voltage applied to the transistor, and ϕ_{ms} represents the work-function difference between the gate metal and the semiconductor.

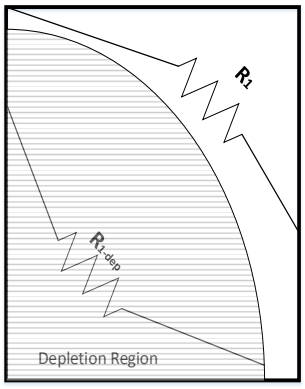

Fig. 5. Resistor model of region 1 [25].

2) Resistances of the region 2 (R_2), 4 (R_4) , and 6 (R_6)

A simplified representation of region 2 is shown in Fig. 6. To facilitate the calculations, several reasonable assumptions are made. First, it is assumed that the depletion regions induced by the p-type windows do not extend into adjacent regions but instead extend only vertically into the drift region. Second, the electric current lines are assumed to be parallel to the surface. The resistances of regions 2, 4, and 6 are calculated using the basic resistance relation given in (3). For this purpose, each region is divided into infinitesimal sections of length dl and thickness T_{ch}, where the resistance of each section, denoted by dR, is determined by the following expression.

$$dR = \frac{R_{sh} dl}{T_{ch}} \quad (9)$$

Both sides of (9) are multiplied by a constant electric current, denoted by I.

$$I \times dR = I \times \frac{R_{sh} dl}{T_{ch}} \quad (10)$$

Integrating along the length of region 2 from L_s to $L_s + L_2$ yields:

$$\int_{V_{S2}}^{V_{E2}} dV = I \times \int_{L_s}^{L_s + L_2} \frac{R_{\text{sh}}}{T_{\text{ch}}}\, dl \quad (11)$$

where, L_s denotes the starting coordinate of region 2, L_2 is its length, and V_{S2} and V_{E2} are the voltages at the beginning and end of region 2, respectively. Solving the integral in (11) gives the potential difference across region 2:

$$V_2 = \frac{R_{sh} \times I}{T_{ch}} L_2 \quad (12)$$

Dividing both sides of (12) by the current I, give the resistance of region 2:

$$R_2 = R_{sh} \frac{L_2}{T_{ch}} \quad (13)$$

Using the same assumptions and procedure, the resistances of regions 4 and 6 can be calculated similarly:

$$R_4 = R_{sh} \frac{L_4}{T_{ch}} \quad (14)$$

$$R_6 = R_{sh} \frac{L_6}{T_{ch}} \quad (15)$$

Here, L_4 and L_6 denote the lengths of regions 4 and 6, respectively. It should be noted that in calculating R_6, the depletion region extended by the drain is assumed to be very small and is neglected.

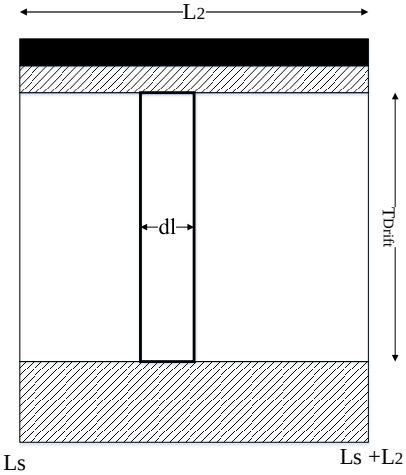

Fig. 6. Simplified schematic of region 2 of the PW-LDMOSFET structure.

3) Resistance of region 3 (R_3) and 5 (R_5)

Fig. 7 shows a simplified schematic of region 3 of the PW-LDMOSFET structure. The depletion region formed below region 3 by the p-type window has a length denoted as T_{dep}. As previously mentioned, it is assumed that this depletion region of p-type windows and the drift region extend only vertically. Similarly, to calculate the resistance of region 3, the region is divided into infinitesimal sections of thickness dl. The resistance of each section is shown by dR and given by:

$$dR = R_{sh}\frac{dl}{T_{ch} - T_{dep}} \tag{16}$$

Here, T_{ch} is the channel thickness. The depletion depth T_{dep} is obtained as:

$$T_{dep} = \sqrt{K(V - V_{bi})} \tag{17}$$

where, V is the potential difference across the junction, and V_{bi} the built-in voltage of the P–N junction. K is a constant parameter that depends on the doping concentrations and material properties of the P–N junction and is obtained as:

$$K = \frac{2\varepsilon_{si}}{q} \times \frac{N_{dr}}{N_{pw} \times (N_{pw} + N_{dr})} \tag{18}$$

Here, ε_{si} is the permittivity of silicon, q is the elementary charge, and N_{dr} and N_{pw} are the doping concentrations of the drift region and the p-type window, respectively.

To calculate the resistance of region 3, T_{dep} is substituted into (16), and both sides of the equation are multiplied by the constant current I. Eq. (19) is then obtained by replacing dV with $I \times dR$ in (16).

$$dV \times \left(T_{ch} - \sqrt{K(V - V_{bi})}\right) = R_{sh} \times dl \times I \tag{19}$$

The resistance of region 3 is obtained by solving the integral along the length of region 3.

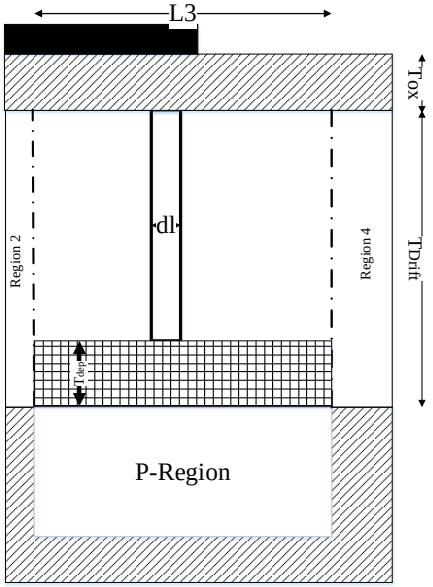

Fig. 7. Simplified schematic of region 3 of PW-LDMOSFET.

$$R_3 = \frac{R_{sh} \times L_3}{T_{ch} - \frac{2}{3} \times \left(\sqrt{\mathrm{K}}\left[\frac{V_4^{3/2} - V_3^{3/2}}{V_4 - V_3}\right]\right)} \tag{20}$$

where V_3 and V_4 are the voltages at the beginning and end of the resistor of region 3, as illustrated in Fig. 4. It should be noted that, for the calculation of the resistor of region 3, the effect of the overlapped gate is neglected.

Due to the similarity between regions 3 and 5, the method for calculating the resistance of region 5 is the same as region 3. By replacing the length of region 5 and the voltage of R_5 according to Fig. 4 in (20), the resistance of region 5 is equal to:

$$R_5 = \frac{R_{sh} \times L_5}{T_{ch} - \frac{2}{3} \times \left(\sqrt{K}\left[\frac{V_6^{3/2} - V_5^{3/2}}{V_6 - V_5}\right]\right)} \tag{21}$$

III. Model Verification

In this section, the proposed model is validated using simulation results obtained from SILVACO-ATLAS. First, the PW-LDMOSFET structure is simulated by SILVACO-ATLAS, while the corresponding circuit model is simulated using SILVACO-SmartSpice [23,24]. The extracted results from both simulations are then compared.

The structural parameters of the proposed PW-LDMOSFET are summarized in Table I, as reported in [21]. In the SILVACO ATLAS simulations, key physical models, including Shockley–Read–Hall (SRH) recombination, Auger recombination, and impact ionization, were incorporated to accurately capture the relevant physical effects influencing the device characteristics [21,23].

TABLE I
Specifications of the PW-LDMOSFET Transistor.

Device Parameters	Value

Gate length (L_G)	5 µm
Channel length (L_{ch})	2 µm
Drift region length (L_{dr})	6 µm
Silicon thickness (T_{ch})	1 µm
Gate oxide thickness (T_{ox})	50 nm
P+ window length	1 µm
P+ window depth	1 µm
P+ window doping concentration	5×10^{18} cm^{-3}
Channel doping concentration	1×10^{17} cm^{-3}
Drift region doping concentration	5×10^{15} cm^{-3}

Fig. 8 shows the drain current versus the drain voltage at different gate voltages for both the PW-LDMOSFET structure and the proposed circuit model. The results confirm the accuracy and reliability of the proposed model in both linear and saturation regions for gate voltages above the threshold voltage.

As observed in Fig. 8, when the drain voltage is 2 V, the device operates in the linear region, whereas at a drain voltage of 5 V, it operates in the saturation region. Furthermore, the results presented in Fig. 9 demonstrate good agreement between the on-resistance predicted by the proposed model and the simulation results in both operating regions. As discussed above, only gate voltages exceeding the threshold voltage are considered, since under the stated assumptions, the proposed circuit model is valid exclusively in the above-threshold operating regime.

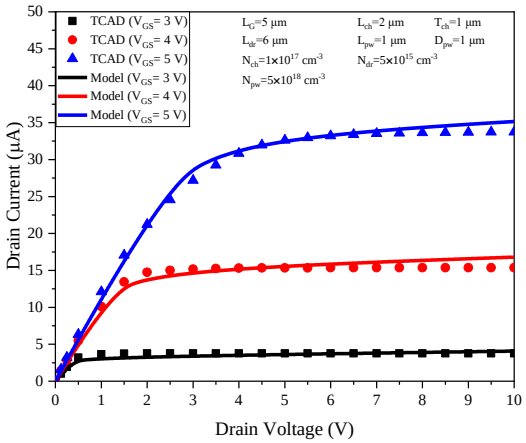

Fig. 8. ID-VDS of the PW-LDMOSFET structure and model at different VGS

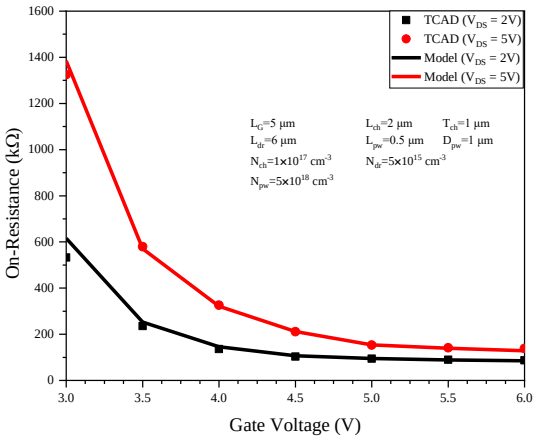

Fig. 9. The On-Resistance of PW-LDMOSFET extracted from ATLAS and Model versus Gate Voltage.

Fig. 10 shows the on-resistance of the PW-LDMOSFET as a function of the drift-region doping concentration. The on-resistance values are calculated at a gate voltage of 4 V.

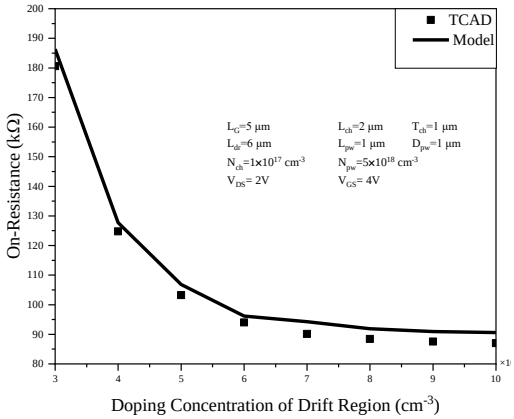

Fig. 10. On-Resistance of PW-LDMOSFET extracted from ATLAS and Model versus Doping of the drift region.

The circuit model proposed in this paper is based on the PW-LDMOSFET structure; however, it can be readily extended to other novel LDMOSFET structures that incorporate p-type windows. This flexibility arises from the method used to calculate the series resistances, where each region is divided into completely separate sections that can be added or removed with minimal modification. Fig. 11 shows the drain current versus the drain voltage when the length of the p-type windows is reduced to 0.5 µm. The results indicate that such changes in the structural parameters do not compromise the accuracy of the proposed model, which remains reliable under these variations.

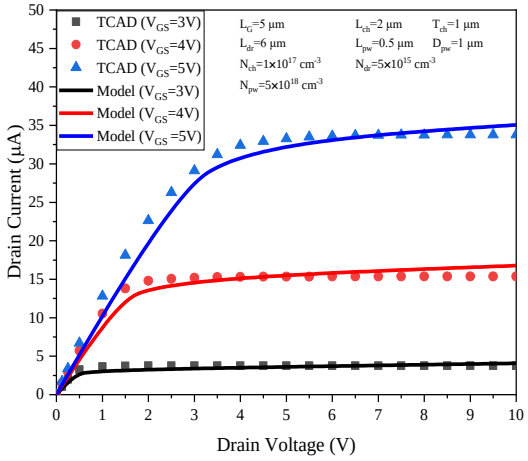

Fig. 11. The ID-VDS of PW-LDMOSFET by Simulation and Model for Lpw= 0.5 µm.

IV. CONCLUSION

A compact circuit model for the PW-LDMOSFET was developed and validated against SILVACO-ATLAS simulations. The model accurately predicts drain current and on-resistance for gate voltages above the threshold voltage. Analytical expressions for the resistances of drift-region sections account for p-type windows and depletion effects. The results demonstrate that the model remains reliable under variations in structural parameters. Its modular formulation

allows straightforward extension to other LDMOSFET designs incorporating p-type windows, enabling efficient circuit-level simulations of power devices.

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CONFLICTS OF INTEREST

The author declares that there is no conflict of interest regarding the publication of this article.

AUTHORS CONTRIBUTION STATEMENT

Ali Shokouhi Shoormasti: Conceptualization, Writing-original draft, Software.

Abdollah Abbasi: Supervision, review & editing.

Ali A. Orouji: Supervision, review & editing.

DATA AVAILABILITY

The data that support the findings of this study are available from the authors upon reasonable request.

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BIOGRAPHIES

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